CHAPTER 3 INTERFACE OPERATION

3.1 RS-232C Interface

Using the RS-232C interface, the HX-20 can transfer data to and from a terminal printer, a personal computer, or other terminal via CX-20 acoustic coupler.

Since the RS-232C interface requires prescribed voltage levels (+3V to +27V for SPACE=logic "0" and -3V to -27V for MARK=logic "1"), the voltages meeting this requirement must be generated from the +5V battery voltage. In the HX-20, +8V and -8V are generated as the power supplies for the RS-232C interface by the built-in regulator. To minimize the power comsumption of the HX-20, this regulator is controlled under software so that it operates only when the RS-232C interface is used.

3.1.1 Operation at power ON

When the P36 of the slave CPU (6301) is set at 'HIGH' level, the pin No. 12 of IC "7E" goes low, causing $\overline{SWL}$ signal to be output. This in turn causes transistor Q2 to turn on. When transistor Q2 is turned on, voltage V_B is supplied to the pin No. 14 (V_{CC}) of the TL497, causing it to operate. The TL497 then starts switching transistor Q11 and generates +8V and -8V. +8V is passed to resistor R22 (5.1KΩ), where the voltage is converted to DTR signal.

By sending this signal to a MODEM, it is possible to confirm that the HX-20 and the MODEM interface have been interconnected properly. The RS-232C interface in the HX-20 employs USART (Universal Synchronous/Asynchronous Receiver/Transmitter) ICs (6B: HD75188) quad line driver and 7B: HD75189 quad line receiver) conforming to the interface standard. Therefore, the RS-232C interface operates according to the same interface standard when a voltage of +8V/-8V is supplied.

3.1.2 Interface circuit

Fig. 3-1 shows the circuit diagram of the RS-232C interface.

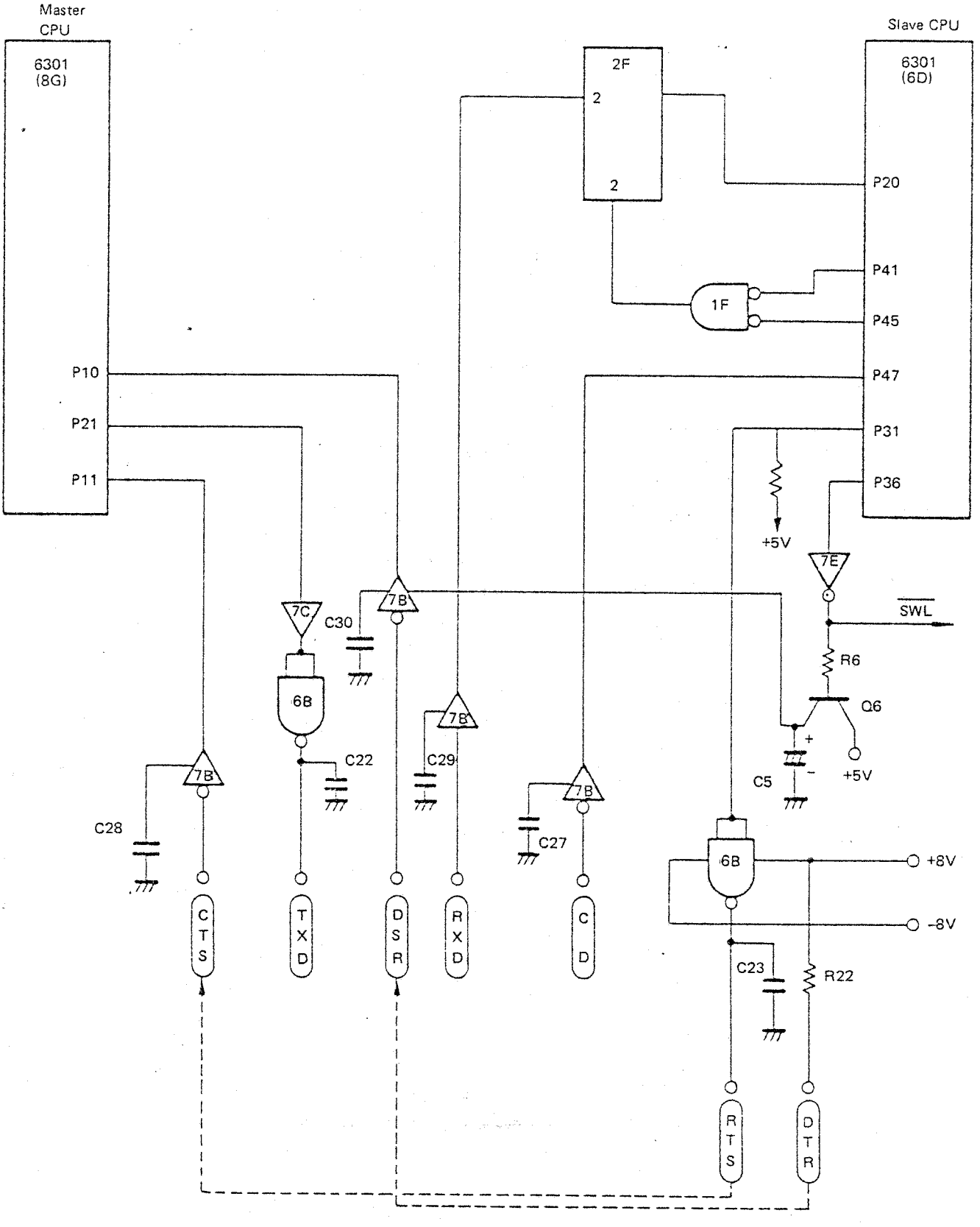


Fig. 3-1 RS-232C Interface Circuit

3.1.3 Operation sequence

In the HX-20, both the master CPU (6301: IC "8G") and slave CPU (6301: IC "6D") control the RS-232C interface operation.
The master CPU controls the data transmission while the slave CPU controls the data reception.
The normal operation of the RS-232C interface is as shown in Fig. 3-2.

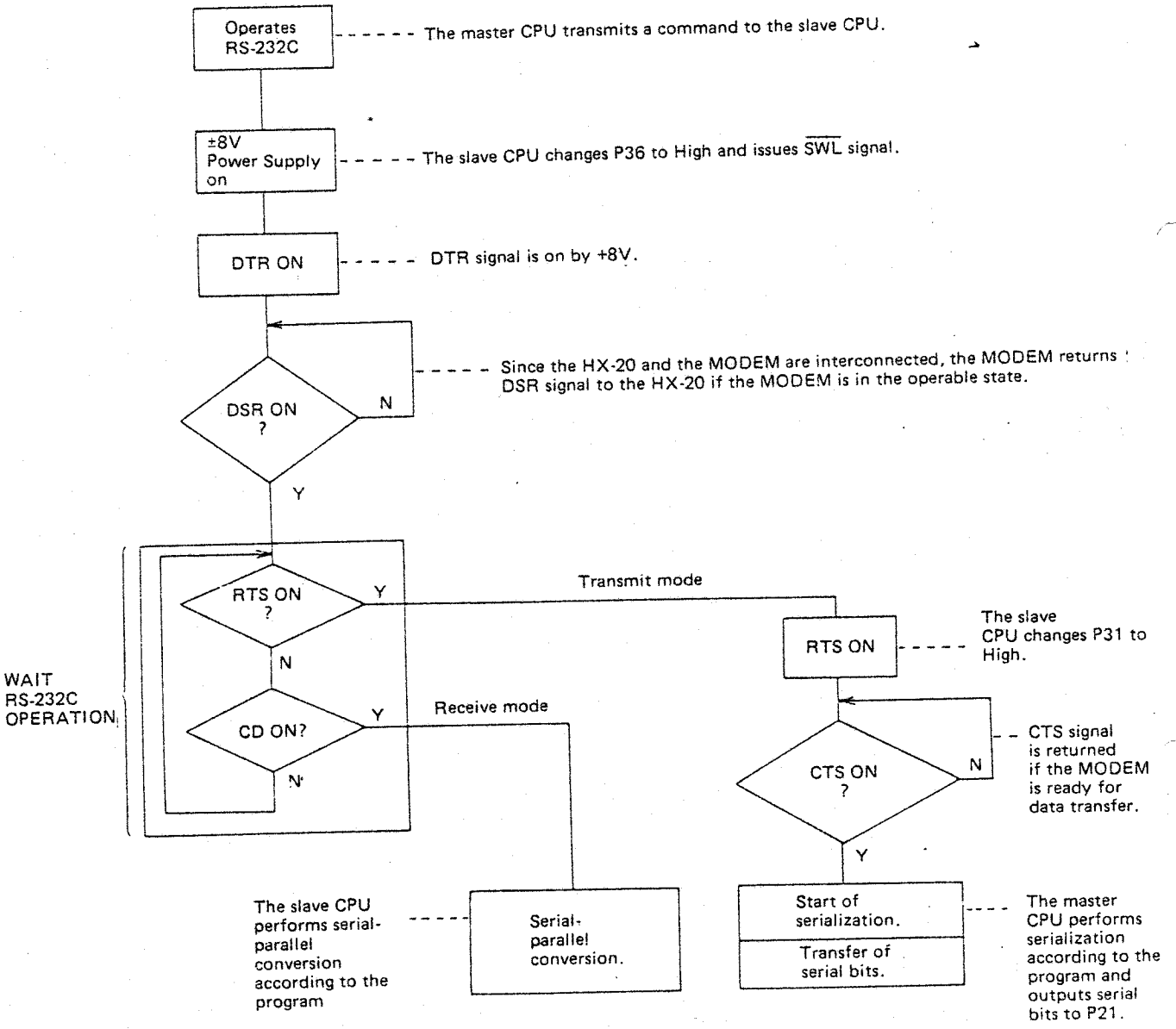


Fig. 3-2 Interface Operation

3.1.4 Operation timing of RS-232C interface

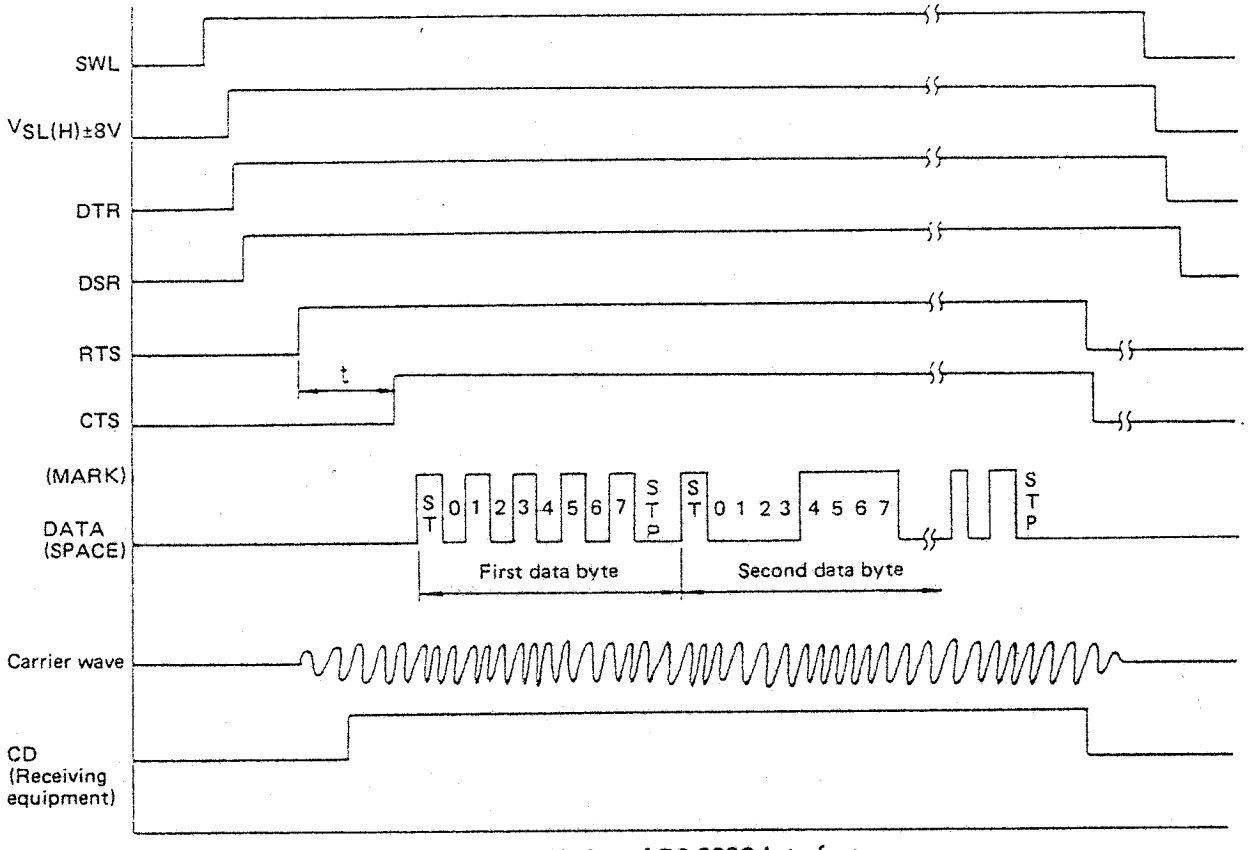


Fig. 3-3 Operation Timing of RS-232C Interface

*: t indicates the delay time until the MODEM becomes ready for data transmission. MODEMs may or may not require this delay time depending on the type.

(1) Signal polarity
  (a) Mark=logic "1" (-3V to -27V)
    : Stop bit
  (b) Space=logic "0" (+3V to +27V)
    : Start bit
(2) Word length
  (a) Start bit: 1 bit
  (b) Data bits: 7 or 8 bits
  (c) Stop bit: 1 bit or more
(3) Bit rate: 110 to 4800 BPS

3.1.5 Operation when a MODEM (coupler) is used

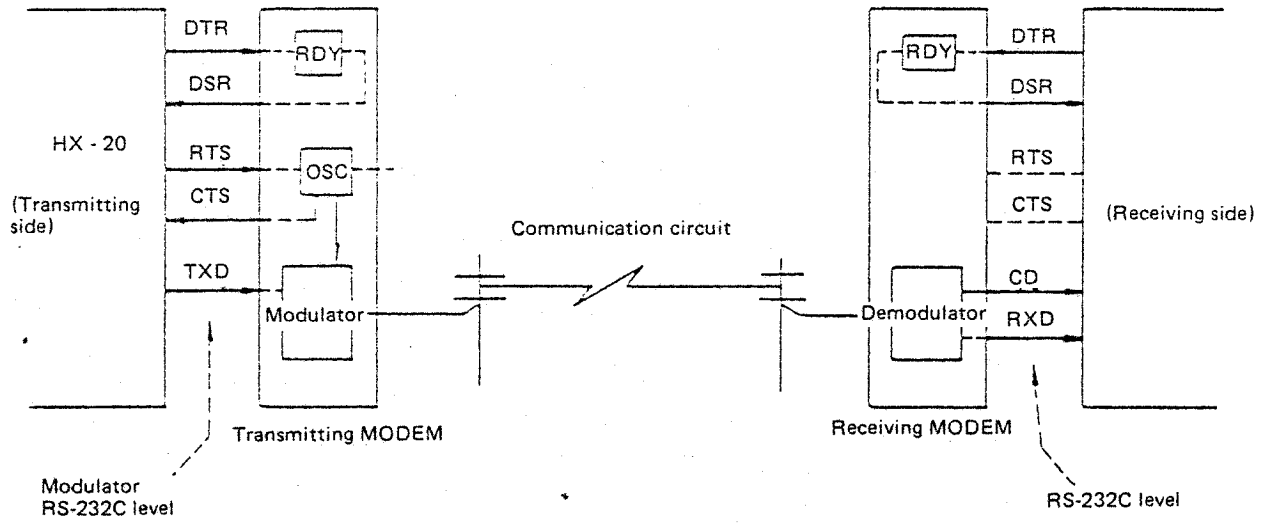


Fig. 3-4 Interface Operation with MODEM

(1) MODEM
MODEM is an acronym for MOdulator/DEModulator. There are 3 modulation modes: Frequency-shift keying (FSK), Phase-shift keying (PSK) and Amplitude modulation (AM).

(2) Operation
The transmitting terminal (HX-20 in Fig. 3-4) outputs a DTR (Data Terminal Ready) signal to check whether or not the MODEM is ready for operation. If the MODEM is operable, the HX-20 receives a DSR (Data Set Ready) signal from the MODEM and then requests the MODEM to transmit data by outputting an RTS (Request To Send) signal to the MODEM if there is any transmit data. When the MODEM receives the RTS signal, it activates the oscillator for a carrier wave and outputs this carrier wave to the transmit data line.
The MODEM also transmits a CTS (Clear To Send) signal to the transmitting terminal after the oscillator output has been stabilized. The time required for output stabilization depends on the characteristics, etc. of the oscillator).
When the receiving MODEM detects the carrier wave on the receive data line, it outputs a CD (Carrier Detect) signal and places the receiving terminal in the standby state for data reception. When the transmitting terminal receives the CTS signal, it converts parallel data into serial data and starts the transfer of data bit by bit to the transmitting MODEM.
The transmitting MODEM modulates the received data bits and transmits them to the transmit data line. As the receiving terminal has been placed in the receiving state by the CD signal, the data modulated and sent by the transmitting MODEM are demodulated by the receiving MODEM and sent to the receiving terminal as digital data. The above MODEM operations are shown in Fig. 3-5, Timing Chart of MODEM Operations.

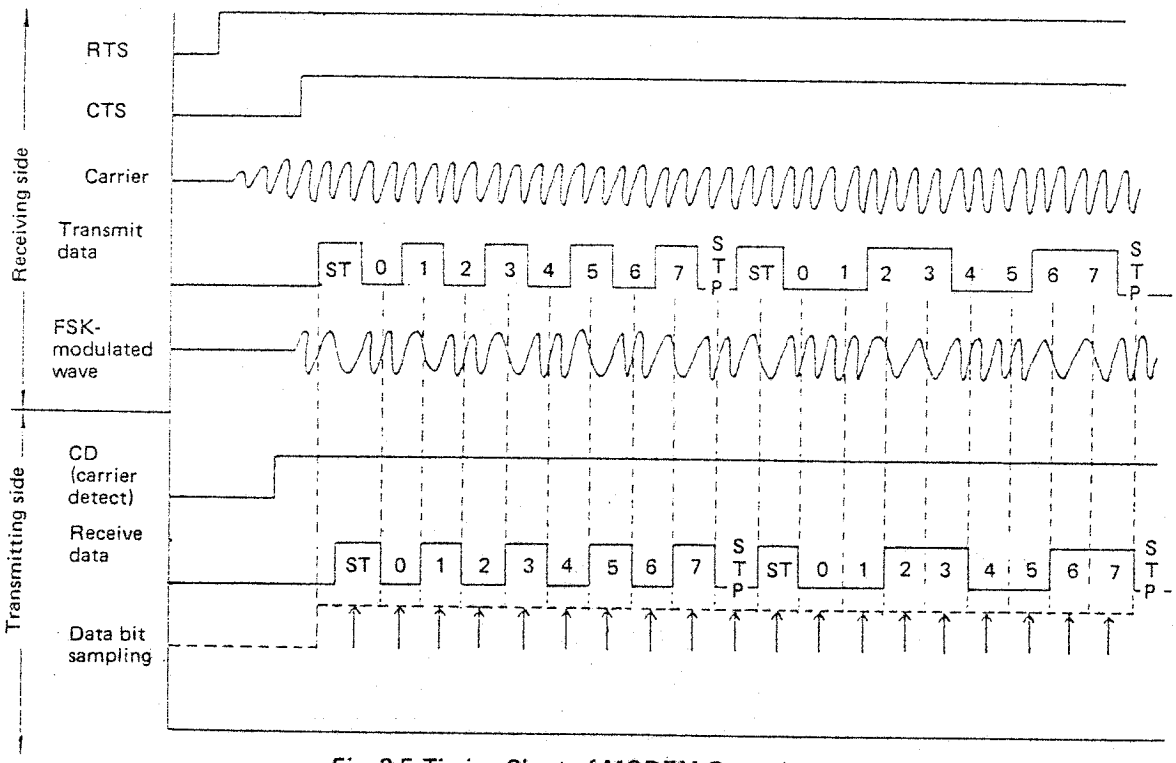


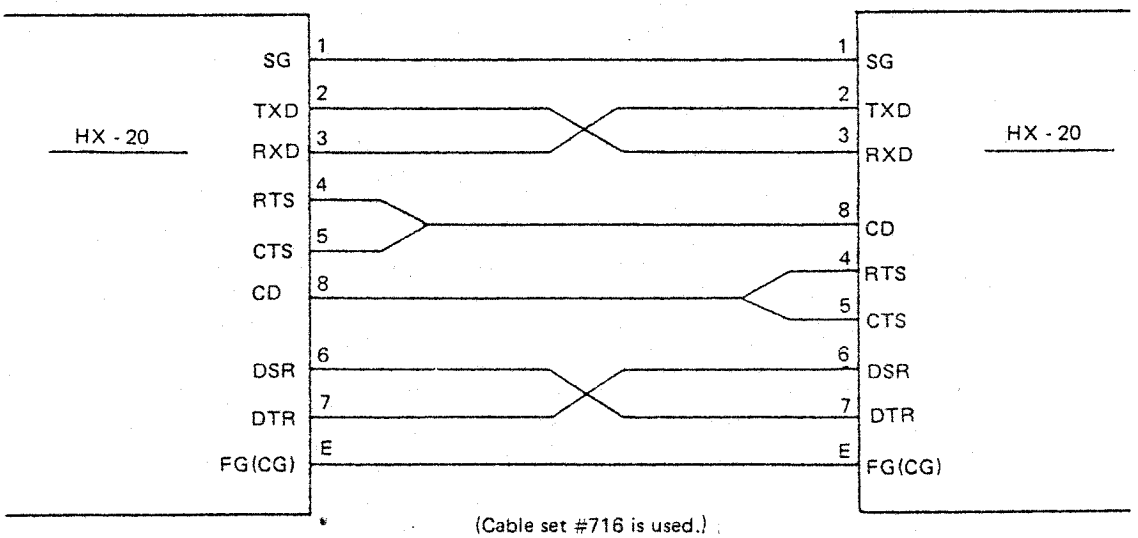
Fig. 3-5 Timing Chart of MODEM Operations

3.1.6 Data transfer between two HX-20 units

The data transmission/reception operation between the two HX-20 units interconnected without a MODEM differs from the normal RS-232C interface operatfon, in that these HX-20 units use the interconnected cables to generate the signals which cannot be normally output without the MODEM.

(1) The DSR and DTR terminals are cross-connected as shown in Fig. 3-6 to turn on the DSR terminal of the receiving HX-20 by the DTR signal of the transmitting HX-20.

(2) The RTS and CTS terminals are connected together within each HX-20 unit, so that a CTS signal is automatically detected upon output of an RTS signal. When the transmitting HX-20 sends this signal to the CD line, the receiving HX-20 enters the receiving state.



(Cable set #716 is used.)

Fig. 3-6 Data Transfer Between Two HX-20 Units

3.1.7 Operation with a terminal printer (exclusive of HX-20)
When an EPSON printer for exclusive use of the HX-20 is to be connected to the HX-20, the printer requires a serial interface (EPSON Cat. No. #8145 with a 2K buffer). When this interface is used, the printer can only receive data from the HX-20. It cannot transmit data to the HX-20.

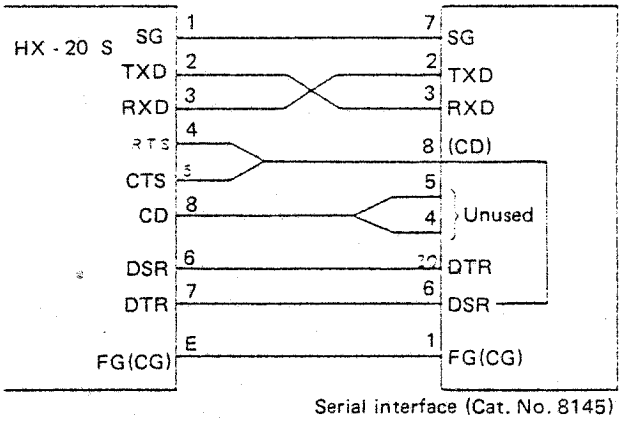


Fig. 3-7

(1) The RTS and CTS terminals are interconnected within the cable on the HX-20, so that a signal from the terminals is connected to the pin No. 8 (CD) of the interface connector on the printer side. Pin No. 8 (CD) and pin No. 6 (DSR) are interconnected on the serial interface board of the printer. Pin No. 6 is connected to the pin No. 7 (DTR) of the interface connector on the HX-20. When the HX-20 outputs a DTR or RTS signal, the RTS, CTS, and DTR terminals of the HX-20, and the CD and DSR terminals of the printer are activated.
(2) The DTR signal of the printer is connected to the DSR terminal of the HX-20 and indicates whether or not the printer is ready for data transfer (when this signal is high, the printer can receive data). The HX-20 thus transfers data to the printer while checking this DSR signal.

3.1.8 RS-232C interface signals
The RS-232C interface signals are controlled by the port addresses of the master or slave CPU and the direction registers corresponding to the port addresses. Since the input/output directions of the interface signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

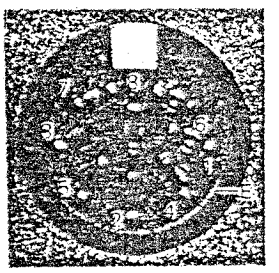
Since the RS-232C interface uses +8V and -8V as the interface signal levels, the port P36 of the slave CPU must be set to High and +8V and -8V must be produced from the battery voltage before using this interface.

Table 3-1 RS-232C Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port (master/slave)	Port address	Control
1	GND	-	Signal Ground	-	-	Negative pole of the built-in battery
2	$\overline{TXD}$	OUT	Transmit Data	P21 (Master CPU)	"0003" Bit 1	Direction register address "0001"
3	$\overline{RXD}$	IN	Receive Data	P20 (Slave CPU)	"0003" Bit 0	Direction register address "0001" (Condition) P41 and P45 of the slave CPU must be LOW. (Address "0007" and Bits 1 and 5) Direction register address "0005"
4	$\overline{RTS}$	OUT	Request to Send	P31 (Slave CPU) (LOW active)	"0006" Bit 1	Direction register address "0004"
5	$\overline{CTS}$	IN	Clear to Send	P11 (Master CPU) (LOW active)	"0002" Bit 1	Direction register address "0000"
6	$\overline{DSR}$	IN	Data Set Ready	P10 (Master CPU) (LOW active)	"0002" Bit 0	Direction register address "0000"
7	$\overline{DTR}$	OUT	Data Terminal Ready	P36 (Slave CPU) (HIGH active)	"0006" Bit 6	Direction register address "0000"
8	$\overline{CD}$	IN	Carrier Detect	P47 (Slave CPU)	"0007" Bit 7	Direction register address "0005"
E	$\overline{CG}$	-	Protective Ground	-	-	This pin is connected to the signal ground via a parallel circuit consisting of a 220KΩ register and a 0.01μF capacitor.

NOTES: 1. Direction registers
Both the master and slave CPUs have the direction registers which correspond to the respective I/O ports and define the input/output directions of the respective I/O terminals as follows.
Bit 1: Output
Bit 0: Input
The bit 1 of port 2 can be used for input or timer output. Thus the port 2 cannot be used as an output port.

2. By setting the port P36 of the slave CPU to High and producing +8V with the regulator, the DTR signal can always be held in the ON state by +8V.



3.2 Serial Interface

As serial interface employs the high-speed data transfer line between the master CPU and the slave CPU, this line is open to external devices as a high-speed serial interface on a time sharing basis. This serial interface allows data transfer at a maximum rate of 38,400 BPS and enables the HX-20 to be connected to a TF-20 floppy disk unit.

3.2.1 Operation control

The IC "4D" (4016) is located between the master CPU and slave CPU. By controlling a gate signal from this IC by the port P22 of the master CPU, the serial line is switched to perform data transfer in the full-duplex transmission system.

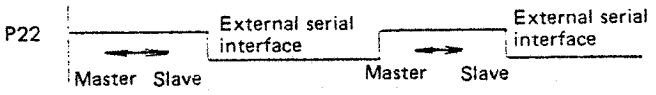


Fig. 3-8 Control of Interface Operation

3.2.2 Interface Operation

The serial interface is structured much simpler than the RS-232C interface, because the former can transfer data without a MODEM, eliminating the need of control signals for the MODEM.

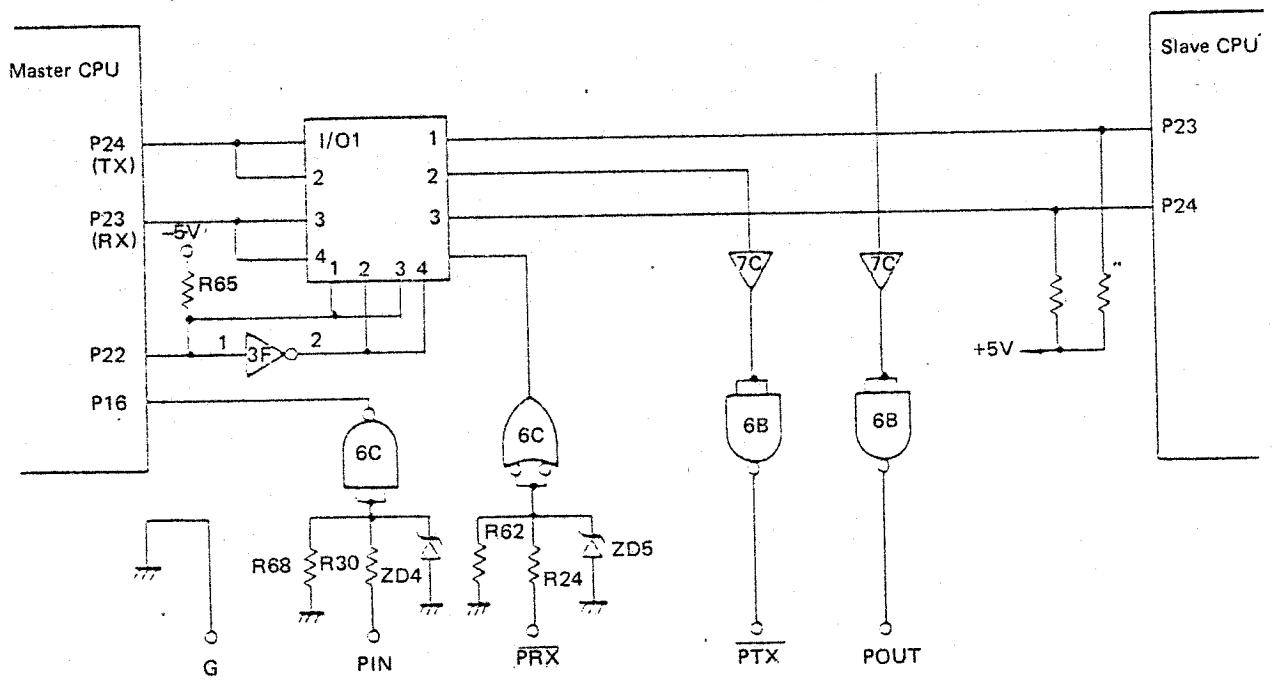


Fig. 3-9 Serial Interface Circuit

(1) Signal levels

The signal levels conforming to the RS-232C standard must be used when data transfer is to be performed between the HX-20 and an external device via the serial interface.

This means that +8V and -8V must be produced at the power supply section before starting the serial interface operation as in the case of the RS-232C interface.

3.2.3 Data transfer between two HX-20 units

The use of cable set #717 allows data transfer between two HX-20 units. The PTX and PRX terminals and the PIN and POUT terminals are cross-connected within the respective cables as shown in Fig. 3-10.

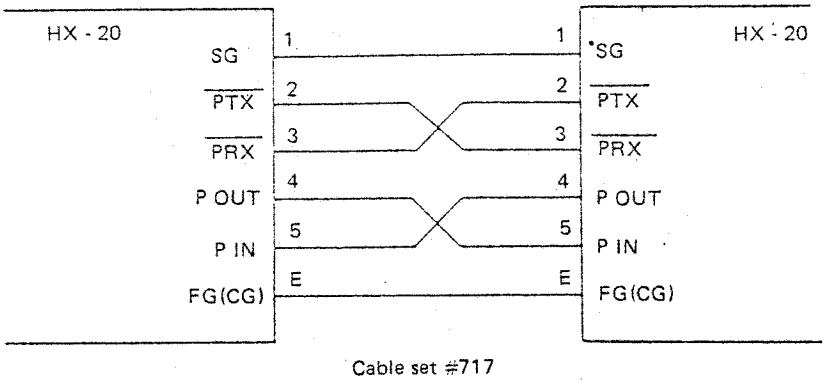


Fig. 3-10 Interconnection of Two HX-20 Units for Data Transfer

3.2.4 Connection with floppy disk units

Cable set #707 is used to connect two TF-20 floppy disk units with the HX-20 in daisy-chain mode. This cable uses two DIN connectors; 5-pin and 6-pin connectors. The pin No. 6 of the 6-pin DIN connector is not used for signal transmission, as it is merely intended for prevention of the incorrect insertion of the DIN connector.

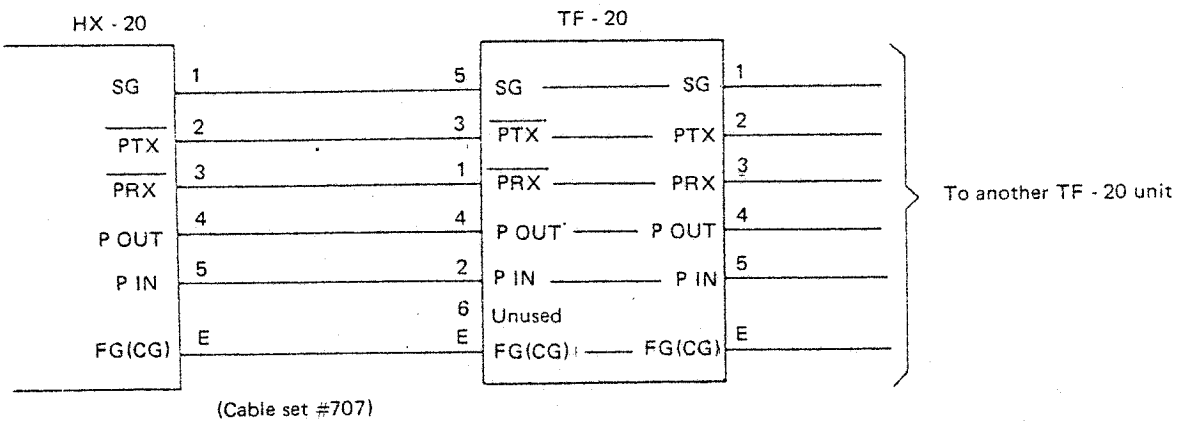


Fig. 3-11 Connection of HX-20 with TF-20

3.2.5 Serial interface signals

Since the serial interface uses +8V and -8V (supply voltages for RS-232C interface) as the interface signal levels, the port 36 (bit 6 of address "0006") of the slave CPU must be set to High and +8V and -8V must be output from the regulator before operating the serial interface. When ±8V is output, the DTR signal of the RS-232C interface is set to ON.

(1) As the input/output directions of the interface signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

(2) Connector: 5-pin DIN connector TC4450

Table 3-2 Serial Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port (Master/slave)	Port address	Control
1	GND	-	Signal ground	-	-	Negative pole of the built-in battery
2	$\overline{PTX}$	OUT	Transmit data	P24 (Master CPU) P22 (Master CPU) (LOW active)	Bit 4 "0003" Bit 2 "0003"	Direction register address "0001" (Condition) The P22 of the master CPU must be at LOW level. P22 controls switching between slave CPU and serial interface.
3	$\overline{PRX}$	IN	Receive data	P23 (Master CPU) P22 (Master CPU) (LOW active)	Bit 3 "0003" Bit 2 "0003"	Direction register address "0001" (Condition) The P22 of the master CPU must be at LOW level. P22 controls switching between slave CPU and serial interface.
4	POUT	OUT	Transmit mode	(Master CPU)	DA5 "0026"	
5	PIN	IN	Receive mode	P16 (Master CPU)	Bit 6 "0002"	Direction register address "0000"
E	CG	-	Protective ground	-	-	This pin is connected to the signal ground via a parallel circuit consisting of a 220KΩ resistor and a 0.01μF cpacitor.

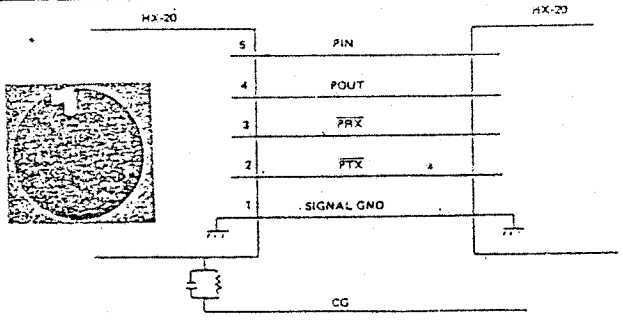


Fig. 3-12 Serial Interface Signals

3.3 External Cassette Interface

The external cassette interface in the HX-20 is used to read or write data (programs) to or from an ordinary cassette tape recorder. The same cassette tape recorder must be used for read/write operations, as the frequency characteristic, tape speed, the position adjustment of the read/write head (i.e., azimuth alignment), etc., of cassette tape recorders differ from one type to another. Note that if a tape written by one cassette tape recorder is read by another recorder, a read error may occur.

3.3.1 Operation control

All the cassette tape recorder operations are controlled by the slave CPU. Cable set #702 is used to connect the HX-20 with the cassette tape recorder.

(1) Motor control circuit

When the "RMT" cable is plugged into the cassette tape recorder and the recorder is placed in the RECORD or PLAYBACK mode, the HX-20 can control the motor of that recorder.

When the slave CPU receives a LOAD or SAVE command, the port P30 of the slave CPU goes Low, causing the anode side of diode D8 in the interface circuit to go Low, and the contact of relay LAD1 in the interface circuit to make. Then, the motor circuit of the cassette tape recorder is activated as shown in Fig. 3-13 and starts rewinding the cassette tape.

When the cassette tape recorder is not in use, the IN signal is pulled up from diode D10 so that the HX-20 accepts no data. However, when the port P30 of the slave CPU goes Low after the motor has been turned on, the IN signal line is also put in the operable state.

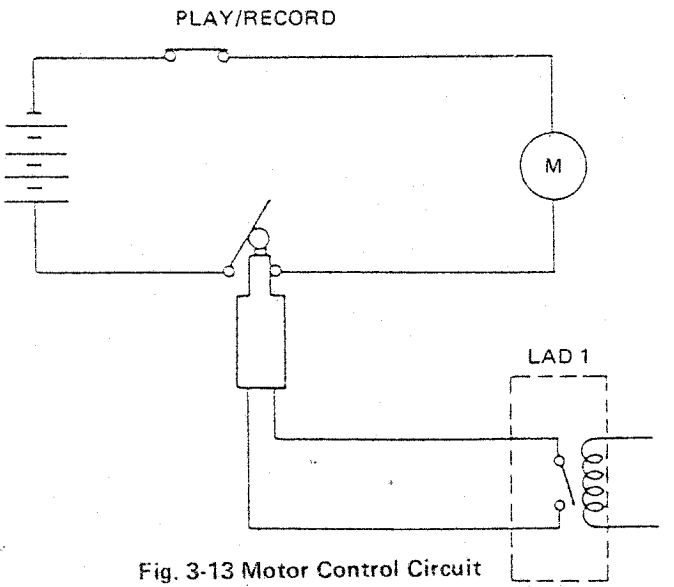


Fig. 3-13 Motor Control Circuit

(2) Data read

For a data read from the cassette tape recorder to the HX-20, the output signal from the cassette tape recorder enters the IN terminal of the interface circuit and is passed through capacitor C36 to cut the DC component of the output signal.
At the same time, the high voltage component due to noise is cut by zener diode ZD6. Then, the AC component thus obtained is supplied to IC "8D", where a threshold voltage is applied to the AC component with capacitor C25 and resistor R55 to shape its waveform as shown by ③ in Fig. 3-14 below. The signal is then passed to the pin No. 9 of IC "8D" and amplified for supply to the slave CPU as a pulse signal.

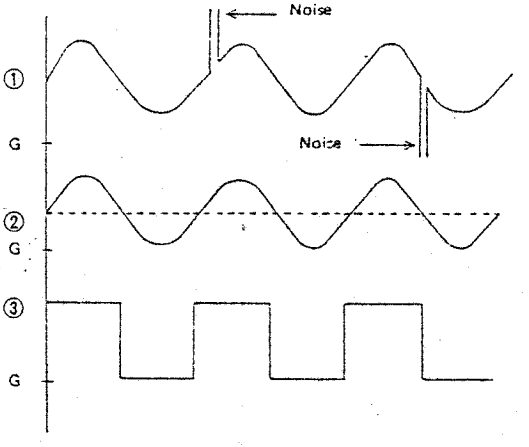


Fig. 3-14 AC Component of Output Signal

(3) Data write

For a data write from the HX-20 into the cassette tape recorder, a pulse signal is output to the cassette tape recorder from the port P33 of the slave CPU via the OUT terminal of the interface circuit. This signal is written into the cassette tape through the Read/Write circuit of the cassette tape recorder.

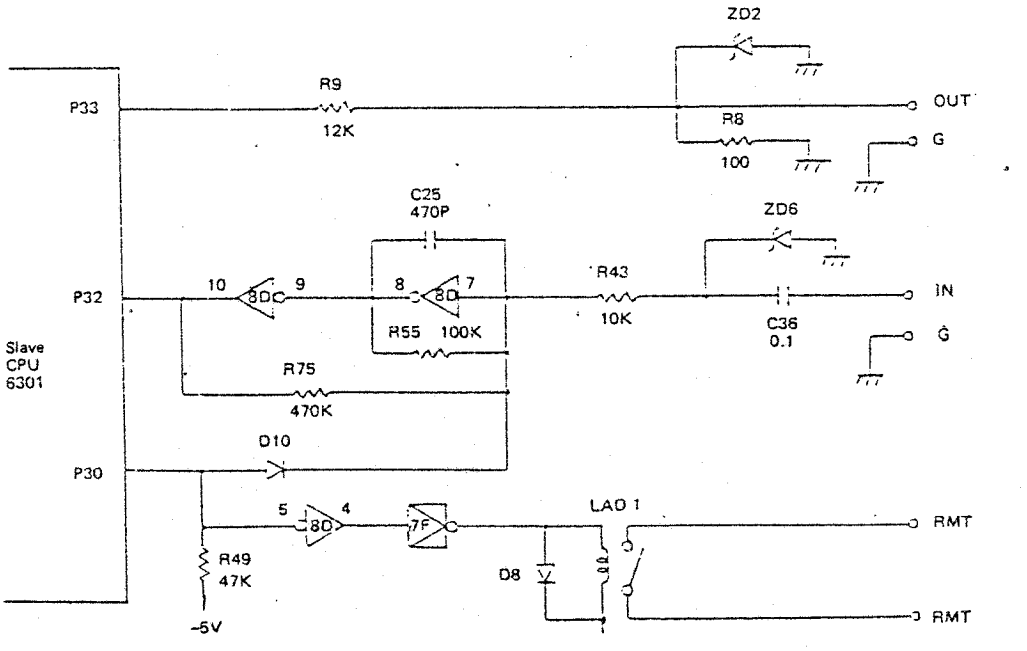


Fig. 3-15 Cassette Interface Circuit

3.3.2 Connection of external cassette with HX-20
Using the exclusive cables (cable set #702), the HX-20 must be connected to the cassette tape recorder as shown in Fig. 3-16.

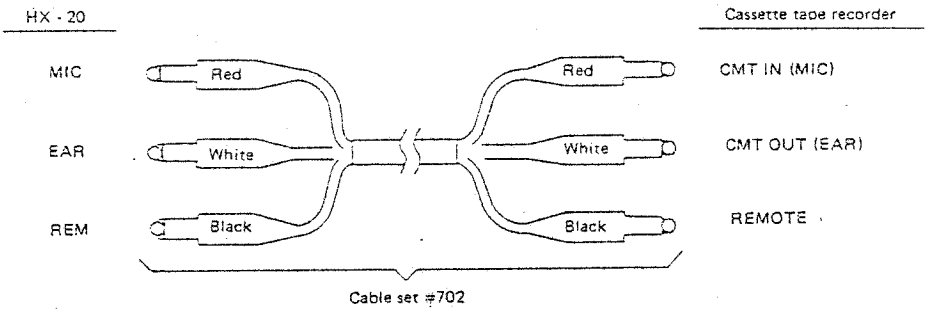


Fig. 3-16 Connection of External Cassette

The REMOTE signal is used for motor control of the cassette tape recorder. To control the motor of/off operation from the HX-20 using this REMOTE signal line, the cassette tape recorder must be set in the RECORD or PLAYBACK mode beforehand.

Note: Do not plug the REMOTE cable into the interface connector when the motor of the recorder is to be controlled manually without using a REMOTE signal.

(1) Read/write signals
The ON-OFF ratio of a read/write signal is 1KHz for ON and 2KHz for OFF.

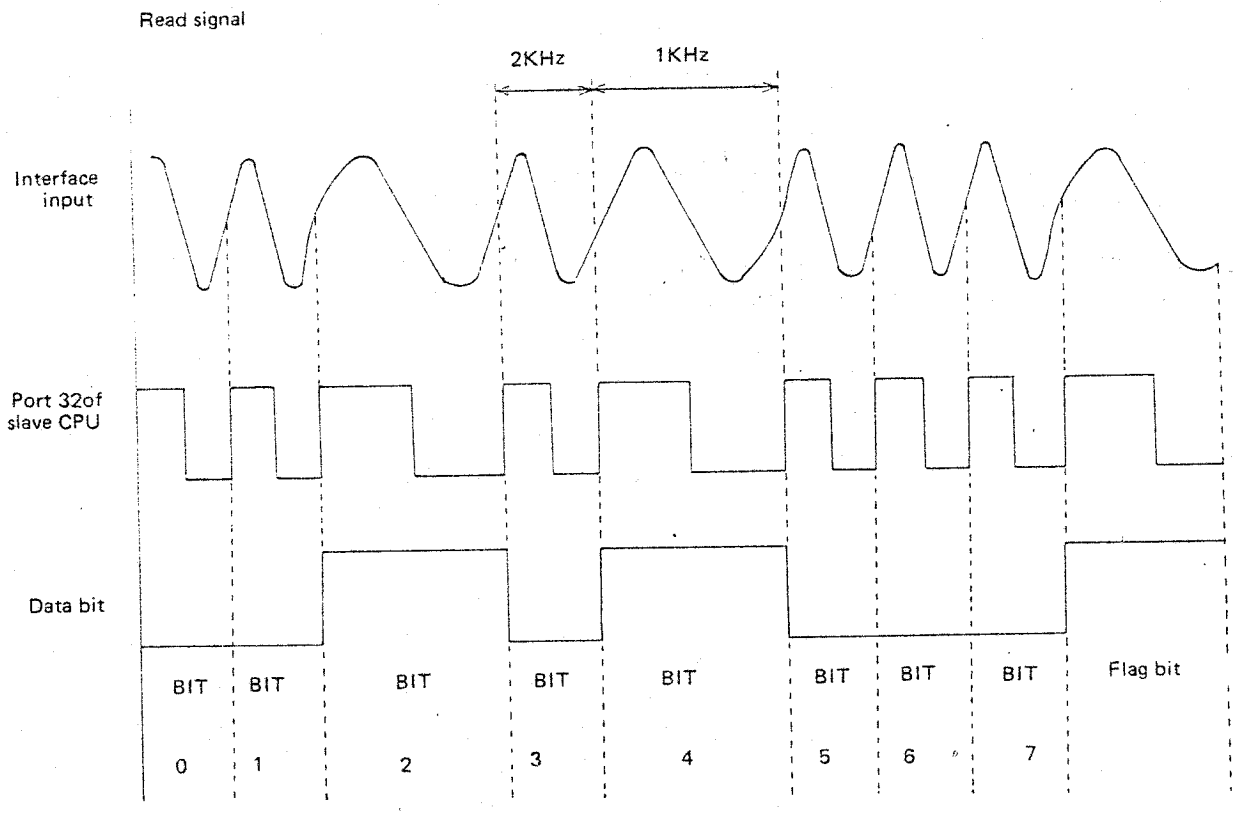


Fig. 3-17 Waveform of Read Signal

Note: A flag bit is required for each byte of data and must always be 1KHz (ON).

3.3.3 External cassette interface signals

As the input/output directions of the external cassette signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

Table 3-3 External Cassette Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port	Port address	Control
W3-1 W3-2	RMT RMT	- -	Remote ON/OFF control	P30 (Slave CPU) (LOW active)	"0006" Bit 0	Direction register address "0004" When port P30 of the slave CPU goes Low, SW3-1 and SW3-2 are interconnected through a 5.1Ω resistor and a relay contact.
W4-1	GND	-	Signal ground			Negative pole of the built-in battery
W4-2	IN	IN	Input data	P32 (Slave CPU)	"0006" Bit 2	Direction register address "0004" (Condition) The port P30 of the slave CPU must be Low.
W5-1	GND	-	Signal ground			Negative pole of the built-in battery
W5-2	OUT	OUT	Output data	P33 (Slave CPU)	"0006" Bit 3	Direction register address "0004"

Notes:

1. A 0.1μF capacitor is connected in series with the IN signal line and an output from this signal line is amplified by the IC via a 10KΩ resistor.
2. The OUT signal is a signal which is output from the port P33 of the slave CPU via a 12KΩ resistor.

3.4 Cartridge Interface (ROM Cartridge or Microcassette)

The cartridge interface is used to read data from the ROM cartridge or microcassette and to write data into the microcassette.

This interface is connected externally from the connector CN8 of the MOSU board via cable set #702 as shown in Fig. 3-18.

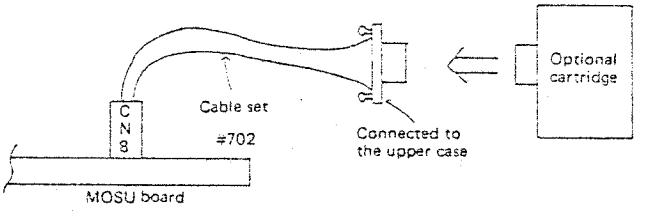


Fig. 3-18 Cartridge Interface

3.4.1 Operation control

Both the master CPU and slave CPU can control the cartridge interface. The type of the cartridge connected to the HX-20 is automatically identified by the 3 signal levels at the pin Nos. 1, 2, and 8 of cable set #702 as shown in Table 3-4.

Table 3-4 Signal Levels for Cartridge Type Identification

Cable set #702	Pin 8	Pin 1	Pin 2
Signal name & Port No. / Cartridge type	MI1 P17 (Master CPU)	SI1 P20 (Slave CPU)	SIO1 P46 (Slave CPU)
ROM cartridge	LOW	LOW	LOW
Microcassette	HIGH	-	-
Reserved	LOW	LOW	HIGH
Reserved	LOW	HIGH	HIGH
Not mounted	LOW	HIGH	LOW

3.4.2 Cartridge interface signals

The input/output directions of all the control signals except MO1 (pin No.5) and MO2 (pin No.6) can be changed by setting the direction registers, because these signals are directly connected to the ports of the master or slave CPU.

The directions of MO1 and MO2 signals are fixed hardware-wise as output only and cannot be changed.

Table 3-5 Cartridge Interface Signals

Pin No.	Signal name	Signal direction	Description	Control Port (Master/slave)	Port address	Control
1 and 2	+5V	OUT	Line voltage	-	-	This signal is supplied upon turning the power switch on.
3 and 4	GND	-	Signal ground			Negative pole of the built-in battery
5	MO1	OUT		(Master CPU)	"0026" DA6	
6	MO2	OUT		(Master CPU) P40 (Slave CPU)	"0026" DA7 "0007" Bit 0	 Direction register address "0005"
7	MI1	IN		P17 (Master CPU)	"0002" Bit 7	Direction register address "0000" This pin is connected to the GND via a 1MΩ resistor.
8	V_B	OUT	Battery voltage	-	-	Positive pole of the built-in battery
9	SIO4	OUT		P42 (Slave CPU)	"0007" Bit 2	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
10	SIO3	OUT		P43 (Slave CPU)	"0007" Bit 3	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
11	SIO2	OUT		P44 (Slave CPU)	"0007" Bit 4	Direction register address "0005"
12	SO1	-		P21 (Slave CPU)	"0003" Bit 1	Direction register address "0001" This pin is connected to the GND via a 100KΩ resistor.
13	SIO1	IN		P46 (Slave CPU)	"0007" Bit 6	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
14	SI1			P20 (Slave CPU) P45 (Slave CPU) (HIGH active)	"0003" Bit 0 "0007" Bit 5	Direction register address "0001" (Condition) The P45 of the slave CPU (bit 5 of address "0007") must be HIGH. Direction register address "0005"

3.4.3 Microcassette interface connector and signals

The microcassette interface signals are connected to connector CN8 of the MOSU board via cable set #701.

(1) Connector CN8

(a) Use: To connect a microcassette drive or a ROM cartridge

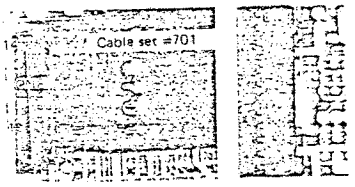


Fig. 3-19 Cable set #701

(b) Number of pins : 14

(2) Interface signals

See Table 3-6.

Table 3-6 Microcassette Interface Signals

CN8 pin No.	#701 pin No.	Signal name Exclusive name	Signal name Generic name	Signal direction	Description
14 13	1	RD/WE	SI1	IN	RD or WE signal is selected according to the value of CLK (pin No. 4) as follows. CLK=0: RD Read data of the microcassette CLK=1: WE Write erase protect signal (WE=0: Insertion inhibit)
12 11	2	CNT/HSW	SIO1	IN	CNT or HSW signal is selected according to the value of CLK (pin No. 4) as follows. CLK=0: CNT Count detection signal CLK=1: HSW Head switch (HSW=0: Head OFF)
10	3	WD	SO1	OUT	Write data to the microcassette
9	4	CLK	SIO2	OUT	Command set clock or RE/WE or CNT/HSW select signal
8	5	CMMND	SIO3	OUT	Serial data output of a command
7	6	PWSW	SIO4	OUT	Power ON/OFF switch
6	7	V_P		-	+5V ((or microccssette drive)
5	8	MCMT/CNT	MI1	IN	When the power is OFF, this signal indicates whether or not the microcassette is connected. (1: Connected 0: Not connected) When the power is ON, this signal causes the count detection signal to be input.
4	9		MO2	OUT	Unused
3	10		MO1	OUT	Unused
2	11	GND		-	Ground
1	12	V_L		-	+5V (for read/write circuit and selector instruction-register)

3.4.4 ROM cartridge

Table 3-7 ROM cartridge Interface Signals

CN8 pin No.	#701 pin No.	Signal name	Signal direction	Description
14	1	SI1	IN	ROM casette judgement input (Always "0")
13	2	SIO1	IN	ROM cassette judgement input (Always "0")
12	3	SO1	-	Unused
11	4	SIO2	OUT	Address counter clear
10	5	SIO3	OUT	ROM power on
9	6	SIO4	OUT	Shift register clear (The register is cleared when this signal is logic "0".)
8	7	V_B	-	Battery voltage
7	8	MI1	IN	Shift register output
6	9	MO2	OUT	Shift register clock input
5	10	MO1	OUT	Counter input (⌐) or shift register SHIFT/LOAD select
4 and 3	11	G	-	Ground
2 and 1	12	+5V	-	Line voltage

3.4.4. Barcode interface

The DATA signal line is fixed hardware-wise for input. Before using this interface, the port 35 of the slave CPU must be set to Low to output +5V.

Table 3-8 Barcode Reader Interface Signals

Pin No.	Signal name	Signal direc-tion	Description	Control port	Port address	Control
1	GND	-	Signal ground	-	-	Negative pole of the built-in battery
2	DATA	IN	Received serial data	P20 (Master CPU) P41 (Slave CPU) (LOW active) P35 (Slave CPU) (LOW active)	"0003" Bit 0 "0007" Bit 4 "0006" Bit 5"	Direction register address "0001" Signal Pin No.3
3	+5V	OUT	Line voltage	P35 (Slave CPU) (LOW active)	"0006" Bit 5	

3.5 Expansion Unit Interface

(1) The expansion unit interface is provided in the HX-20 for extension of RAM and ROM memories. To this interface, 16 address lines and 8 data lines are parallelly output, as well as the $\overline{R}/W$ signal is output so that the master CPU can directly access the extended RAM or ROM memory by selecting an appropriate memory bank. In addition, line voltage V_L (+5V), backup voltage V_C (+3V/+5V) and battery voltage V_B are output to the interface so that the circuitry of the expansion unit can be driven with the built-in power supply of the HX-20 alone.

(2) This interface also has other signal lines such as NMI, INT, and EX interrupt signals and bank select signal ROM E. Therefore, it allows the HX-20 to mount units other than the expansion unit.

3.5.1 Operation control

(1) Since the ROM/RAM in the expansion unit and the ROM in the HX-20 share partially the same memory addresses, switching of the memory banks is a must. To switch the memory banks, I/O addresses "0030" through "0033" are used. The ROM E signal is a signal used for this purpose. This signal is normally High. Once the ROM or RAM memory in the expansion unit is specified (by output of address "0030" or "0032"), ROM E goes Low and the ROM selector (IC "15D") in the HX-20 is placed in the non-operating state, causing 40K bytes of addresses "6000" through "FFFF" to be inaccessible.

(2) After the bank selection, the master CPU directly controls the expansion unit using the address and data lines as in the case of the internal ROM or RAM.

3.5.2 Interface connector and signals

(1) Connector CN7

(a) Use: To connect the control signals and data bus lines to the expansion unit

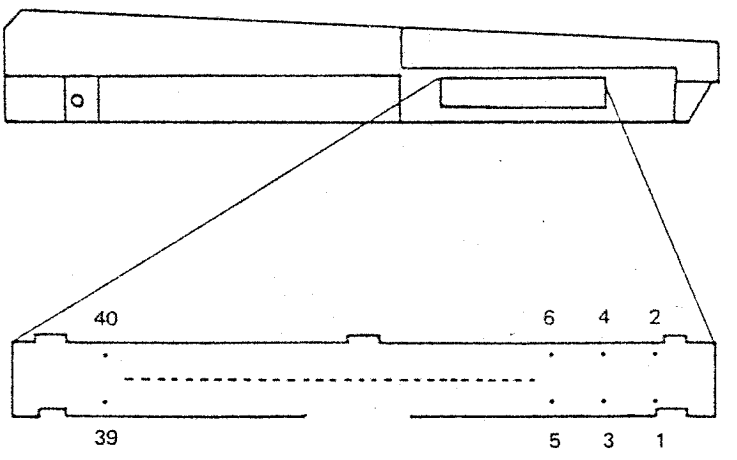


Fig. 3-19 Interface Connector CN7

(b) Number of pins: 40

(2) Interface signals

Table 3-9 Expansion Unit Interface Signals

Pin No.	Signal name	Signal direction	Description
1	VB	-	+5V
2	$\overline{\text{NMI}}$	-	Unused
3	+5V	-	Logic voltage
4			
5	DATA7	IN/OUT	Data line 7
6	DATA6	IN/OUT	Data line 6
7	DATA5	IN/OUT	Data line 5
8	DATA4	IN/OUT	Data line 4
9	DATA3	IN/OUT	Data line 3
10	DATA2	IN/OUT	Data line 2
11	DATA1	IN/OUT	Data line 1
12	DATA0	IN/OUT	Data line 0
13	$\overline{\text{IOCS}}$	OUT	I/O chip select
14	V_C	-	RAM backup voltage
15	ADDR0	OUT	Address line 0
16	ADDR1	OUT	Address line 1
17	ADDR2	OUT	Address line 2
18	ADDR3	OUT	Address line 3
19	ADDR4	OUT	Address line 4
20	ADDR5	OUT	Address line 5

Pin No.	Signal name	Signal direction	Description
21	ADDR6	OUT	Address line 6
22	ADDR7	OUT	Address line 7
23	ADDR8	OUT	Address line 8
24	ADDR9	OUT	Address line 9
25	ADDR10	OUT	Address line 10
26	ADDR11	OUT	Address line 11
27	ADDR12	OUT	Address line 12
28	ADDR13	OUT	Address line 13
29	ADDR14	OUT	Address lin3 14
30	ADDR15	OUT	Address line 15
31	R	OUT	Reset
32	$\overline{\text{R}}$/W	OUT	Read/write
33	$\overline{\text{R}}$ (RAM)	OUT	RAM reset
34	E	OUT	ENABLE signal
35	ROM E	IN	ROM ENABLE
36	$\overline{\text{INTEX}}$	IN	External interrupt signal
37	GND	-	Signal ground
38			
39	CG	-	Chassis ground
40			

Description of each interface signals follows:

V_B : This signal is output from the position terminal of the built-in battery. A voltage of +4V to +6V is normally output from the built-in battery via fuse F1 (5A) regardless of the ON/OFF state of the power switch.

NMI: Non-maskable interrupt signal. Upon completion of a command under execution, the contents of the program counter, index register, etc. are saved to the stack area, a vector address is generated and then program control is transferred to the NMI service routine.

+5V: Line voltage. +5V is supplied only while the power switch is being turned on.

DATA0~ DATA7: 8 parallel data lines. These signals indicate the respective I/O data codes. In Expanded Multiplex mode, these signals can also be used as the 8 low-order bits (ADDR0 through ADDR7) of an address. Each data line is connected to the GND via a 1MΩ resistor (RM-7).

$\overline{IOCS}$: $\overline{A7}$~$\overline{A15}$ address signal. This signal is used as follows.
(1) To enable the accessing of the real-time clock RAM (HD146818) when the address is 004XH (X=0~D). (In this case, the CHIP ENABLE terminal of the HD146818 is set to on.)
(2) To disable the accessing of low-order addresses 0000H through 07FFH of the external RAM in the HX-20. In this case, CE2 signal for RAM at location "13C" is not output.
(3) To enable I/O chip selection when the address is 002XH (X=0, 2, 6, 8, A, or C).

V_C: C-MOS RAM backup voltage. Approx. +3V is output when the power switch is turned off. The effective output current is 40mA max.

ADDR0~ ADDR15: 16 parallel address lines. These signals are used to address the peripheral devices (RAM and ROM, etc.) connected to the master CPU. In expanded Multiplex mode, the 8 low-order bits (A0 through A7) of an address are also used as data lines D0 through D7.

$\overline{R}$: Reset signal line. This signal is output only when power is applied or when the RESET switch is pressed.
NOTE: This signal is the same as the Reset signal of the master CPU.

$\overline{R}$/W: $\overline{Read}$/Write signal. This signal is an inversion of the R/$\overline{W}$ signal of the master CPU. The signal inversion is performed by IC "3F" (TC40H004).

R (RAM): Reset signal line. This signal is output only when power is applied or when the RESET switch is pressed.
NOTE: The Reset signal of the master CPU is the same as the R (RAM) signal which is output via IC "7C" (TC4049UBP).

E: E (ENABLE) signal of the master CPU. This signal serves as a system clock (614.6 KHz) for external devices.

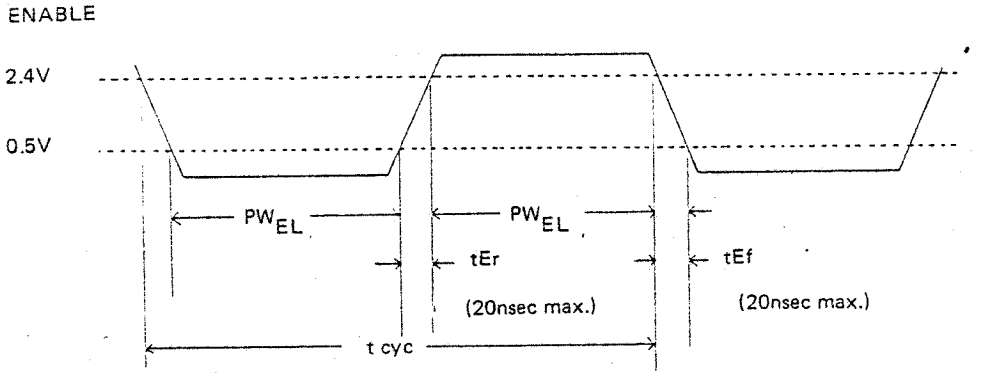


Fig. 3-20 ENABLE signal

ROM E: ROM ENABLE. This signal controls the output of the selector (IC "15D") in the internal ROM (locations 15E through 11E) and is pulled up by +5V line voltage via a 100KΩ resistor (R64) in the control circuit.
When the ROM E signal goes Low, selection of the internal ROM is disabled, since the CE (Chip Enable) signal is not output to the internal ROM.

INTEX: External interrupt signal. This signal serves as an interrupt request ($\overline{IRQ}$) signal to the master CPU and is pulled up by +5V line voltage via a 100KΩ resistor (R70) in the control circuit.

GND: Signal ground. This pin is connected to the negative pole of the built-in battery.

CG: Chassis ground

3.5.3 Timing chart of interface signals
See Fig. 3-2 for the timing chart of the respective interface signals.

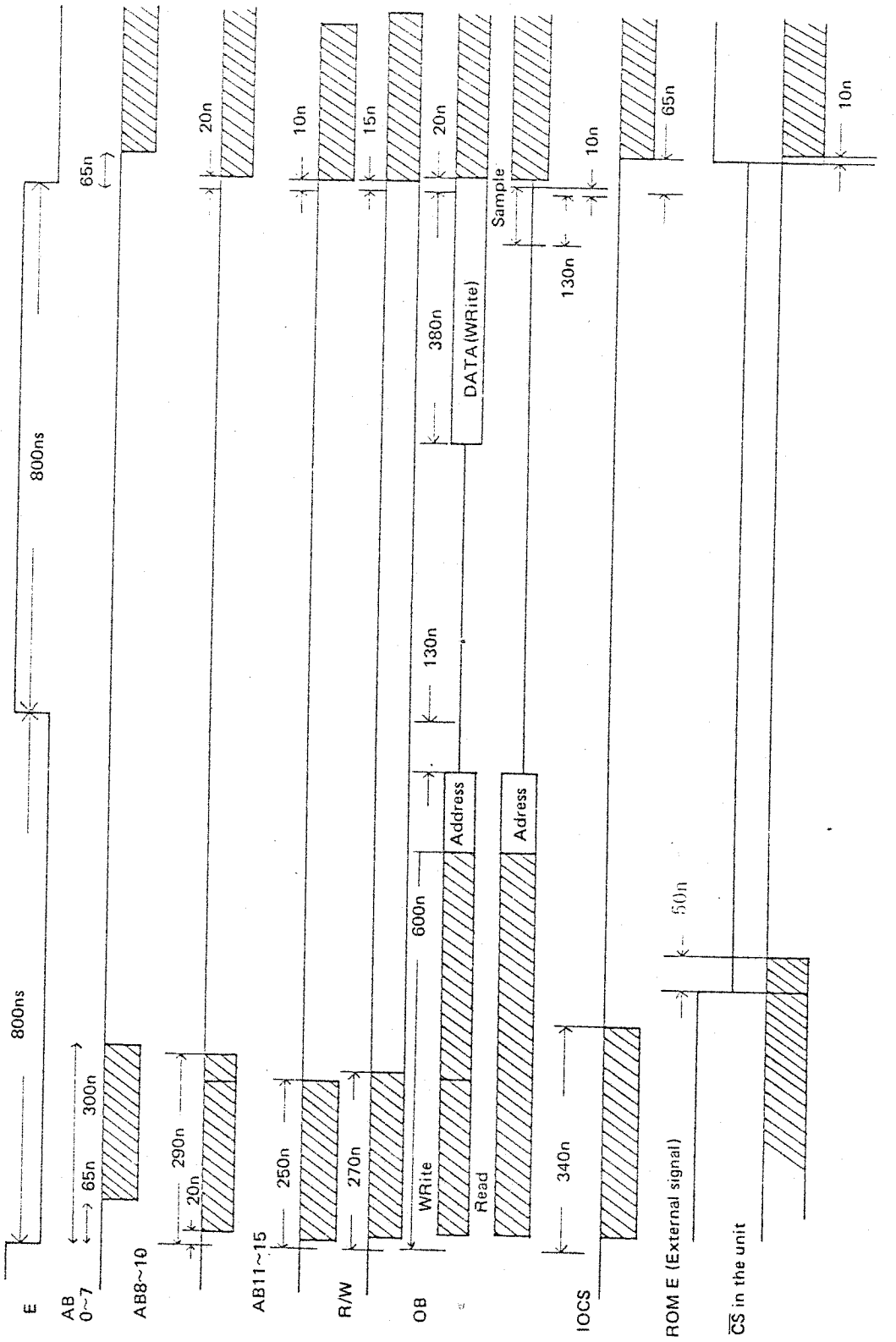


Fig. 3-21 Timing Chart of Expansion Unit Interface Signals