# Part I FIRMWARE

CONTENTS (FIRMWARE)

CHAPTER 1 GENERAL DESCRIPTION

# CHAPTER 1 GENERAL DESCRIPTION

## 1.1 PINE System Configuration

### 1.1.1 General

The PINE is centered on a C-MOS Z-80-compatible microprocessor. Its main memory consists of 64K bytes of RAM and up to 96K bytes of ROM. These RAM and ROM are used alternatively using a bank switching technique.

The PINE also has a 4-bit C-MOS 7508 processor, as its slave CPU, which is used to control the keyboard, clock, and power units. In addition to these processors, the PINE employs three types of semicustome gate array (GA) ICs, namely, the main memory control GA, interrupt controller GA, and I/O control GA.

Power to the PINE is supplied from the NiCd power battery, Mn dry batteries, or AC adapter.

Figure 1.1.1 shows the PINE hardware configuration.

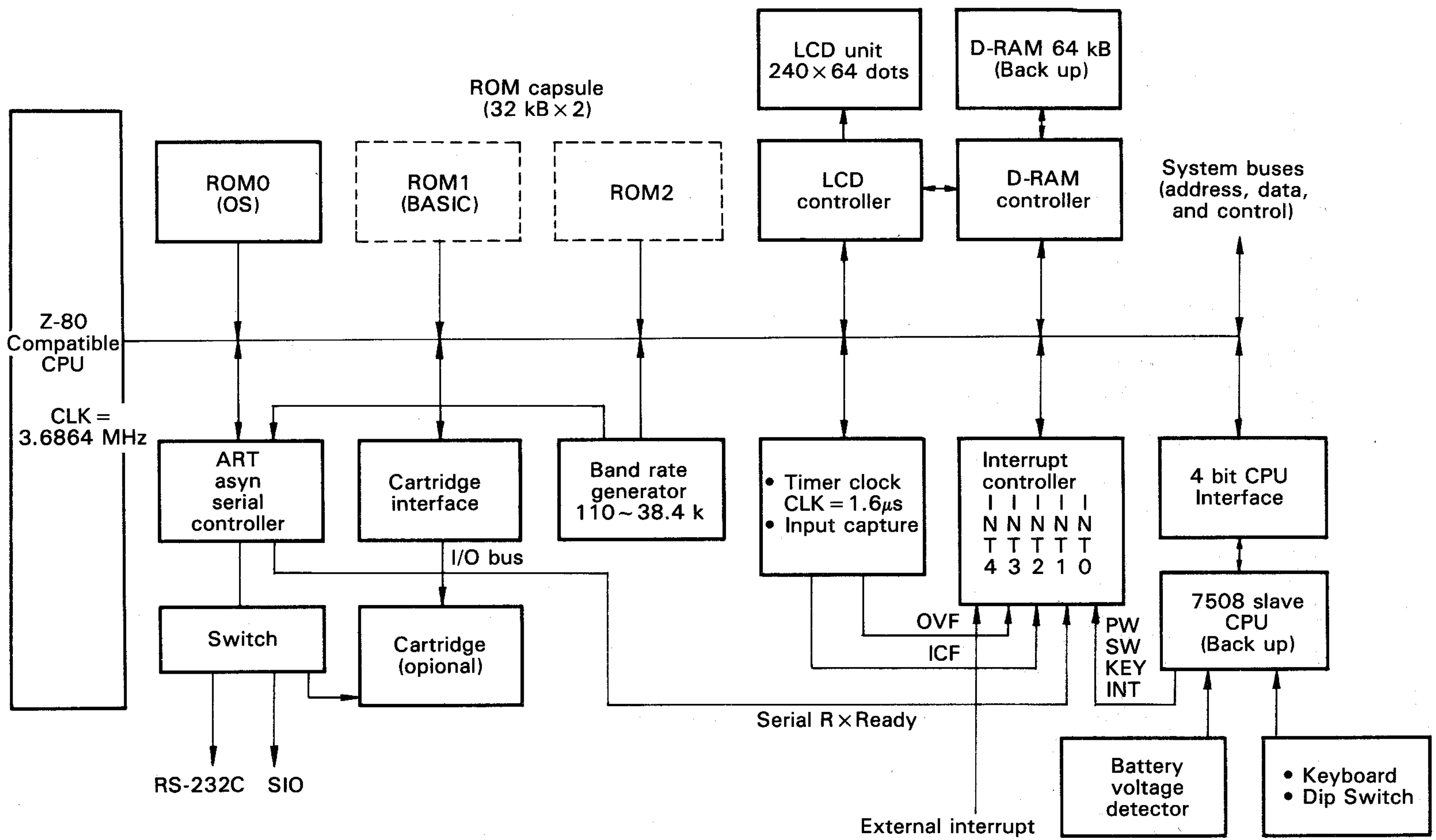



Figure 1.1.1 Hardware Configuration

### 1.1.2 Hardware Description

#### 1.1.2.1 CPU

The PINE main CPU is a Z-80-compatible C-MOS CPU uPD70008 running at a basic clock rate of 3.6864 MHz. The CPU is put into the sleep state by the HALT instruction to save power energy.

#### 1.1.2.2 Main memory

ROM: 96K bytes (maximum): 256K-bit C-MOS mask ROM x 3
RAM: 64K bytes: 64K-bit C-MOS D-RAM x 8
Memory reads, writes, and refreshing are controlled by the D-RAM controller GA. The RAM memory is battery backed up and its data is sustained even when power switch is turned off.

#### 1.1.2.3 7508 (slave CPU)

The slave CPU is a 4-bit C-MOS 7508 microprocessor equipped with the sleep and timer functions. It runs on a basic clock of approximately 270k Hz. The 7508 is battery backed up and can continue its operation even when power is shut down. The 7508 is used to monitor the battery voltage and temperature. Its primary functions are to:

- Provide the timer/clock functions.
- Sense D-RAM temperature (at power-off time)
- Turn power on and off.
- Set and reset the system.

#### 1.1.2.4 GAPNDL (Main memory control GA)

The GAPNDL controls the operations (read, write, and refresh) of the 64K-byte DRAMs as well as the 240 x 64 dots LCD unit.

#### 1.1.2.5 GAPNIT (Interrupt/timer control GA)

The GAPNIT serves as:

- Interrupt controller
- Timer/baud rate generator (with input capture feature)
- Interface to the 4-bit 7508 CPU
- ROM/DRAM address decoder and DRAM address multiplexer

#### 1.1.2.6 GAPNIO (I/O control GA)

The GAPNIO serves as:

- Asynchronous Receiver Transmitter (ART)
- Centronics interface
- Cartridge (CTG) interface
- Serial I/O interface (SIO)
- RS-232C interface
- LED and buzzer interface

#### 1.1.2.7 SIO Interface

The SIO interface specifications are given below.

| | |
|---|---|
| Level: | RS-232C level ±5 V |
| Baud rates | 110, 150, 200, 300, 600, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 75 bps |
| Start bits: | 1 bit |
| Stop bits: | 1 or 2 bits |
| Parity: | Even/odd or no parity |
| Communication mode: | Full duplex |
| Error checking: | Parity, framing, and overrun errors |

The ART in the GAPNIO is used.

#### 1.1.2.8 RS-232C Interface

The RS-232C interface specifications are given below.

| | |
|---|---|
| Level: | RS-232C level ±5 V |
| Baud rates: | Same as for SIO. |
| Start bits: | Same as for SIO. |
| Stop bits: | Same as for SIO. |
| Parity: | Same as for SIO. |
| Communication mode: | Same as for SIO. |
| Error checking: | Same as for SIO. |

The ART in the GAPNIO is used.

#### 1.1.2.9 Keyboard

There are two types of keyboards for the PINE: standard and item keyboards.

| | |
|---|---|
| Standard keyboard: | 72 keys (66 keys plus 6 switches) |
| Item keyboard: | 58 keys (55 keys plus 3 switches) |
| Contact type: | Mechanical contacts |
| Features: | N-key rollover and auto-repeat features<br>Programmable repeat interval<br>7-character buffer<br>Stop-key only mode |

#### 1.1.2.10 LCD

The PINE is provided with a 1/64-duty, 240 x 64 dot matrix LCD unit. The LCD drivers are:

| | |
|---|---|
| X: | SED 1120 x 4 |
| Y: | SED 1130 x 1 |
| Drive voltage: | 10 to 18 volts; view angle is adjustable with a potentiometer. |
| VRAM area: | 2K bytes |
| Display mode: | Dot image (no character generator) |
| Scrolling: | Vertical dot scrolling |

#### 1.1.2.11 Buzzer

The PINE has a piezo-electric buzzer. The buzzer input is obtained by ORing the audio signal from the cartridge interface with the SP signal from the CPU. The buzzer is disconnected when an ear plug is plugged into the external loudspeaker jack.

#### 1.1.2.12 ROM capsule

The PINE can accommodate either 8K-, 16K-, or 32K-byte ROM (maskable or programmable) capsules. These ROM devices have different pin assignments as listed below.

| Pins \ ROM | 61364 | 613128 | 613256 | 27C64 | 27C256 |
|---|---|---|---|---|---|
| 27pin | OE1* | OE1* | A14 | $\overline{PGM}$ | A14 |
| 26pin | OE2* | A13 | A13 | NC | A13 |
| 22pin | OE0* | OE0* | OE0 | $\overline{OE}$ | $\overline{OE}$ |
| 20pin | CS* | CS* | CS* | $\overline{CS}$ | $\overline{CS}$ |
| | Maskable | | | P-ROM | |

Asterisks identify mask-programmable ROMs.

OE0* and CS* must be active low. For 61364, *E1* must be active high and *E2* must be active low. For 613128, OE1* is don't care or must be active low. When OE1* is set to active low, jumper J4 or J5 to side B.

## 1.2 Address Map

The PINE has four types of memory:
1) DRAM (64K bytes)
2) ROM1
3) ROM2
4) ROM3
5) External memory

DRAMs make up a 46K bytes of system RAM memory and are controlled by gate array GAPNDL. ROM1 is used to store the operating system and ROM2 and ROM3 to store application programs. Both have a maximum capacity of 32K bytes (may also be used as 16K- or 8K-byte ROM). The external memory refers to the memory which is installed in the external expansion box and connected to the main unit through the system bus. The main unit does not know whether it is made up of ROM or RAM devices.

A 4-bit bank switch (BANKR bits 7-4 for BANK0 through BANK3) is provided for memory management. This switch is used in conjunction with the address inputs to address the memory. Figure 1.2.1 shows the relationship between BANK3 through BANK0 and their address spaces.

The memory devices installed in the main unit are all controlled by gate array GAPNIT. GAPNIT issues a Select (enable) signal to the memory in the main unit when $\overline{\text{MEN}}$ from the external expansion box is 0 and disables the main unit memory when $\overline{\text{MEN}}$ is 1.

$\overline{\text{MEN}}$ is held at the 0 level when no external expansion box is installed. If an external expansion box is installed, all memory is controlled by the external expansion box.

The external expansion box a bank signal for memory management (different from those generated by GAPNIT and assigned a 1-level higher priority) which is used with the address inputs to determine whether the main unit memory or external memory is to be used.

When using the main unit memory, the external expansion box sets $\overline{\text{MEN}}$ to 0 to disable the external memory and leaves the main memory addressing to GAPNIT's control. When using the external memory, it sets $\overline{\text{MEN}}$ high to disable the memory in the main unit. The GAPNIT does nothing for external memory addressing.

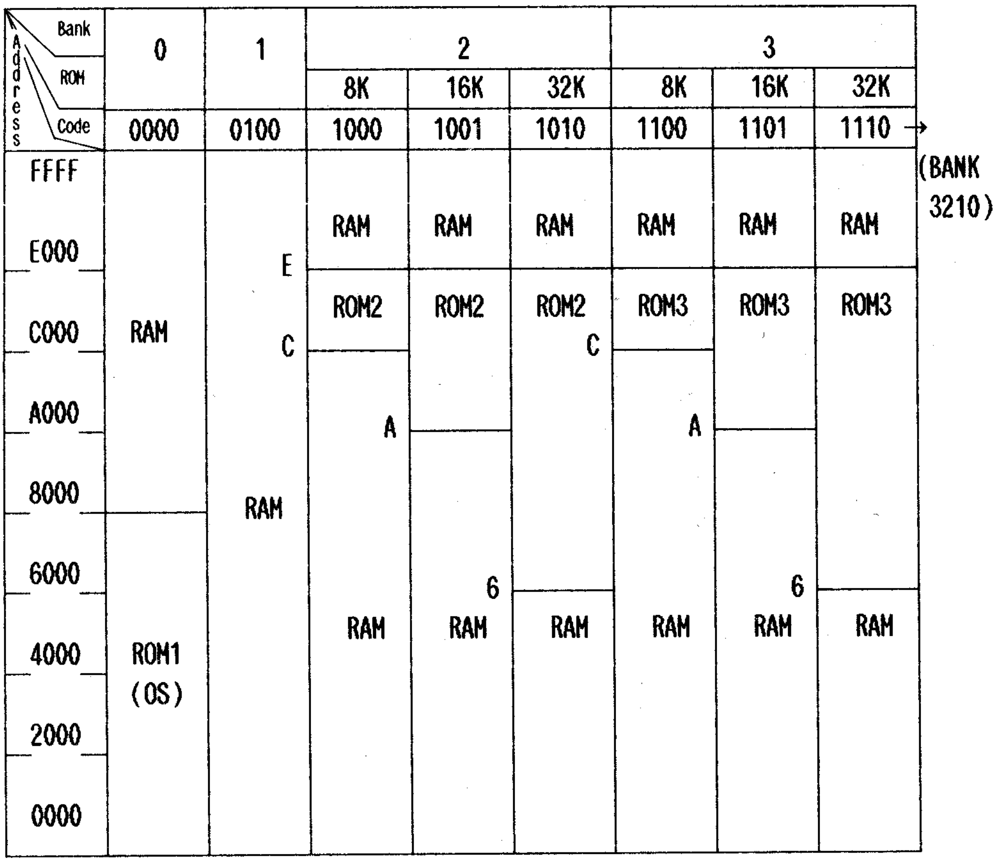
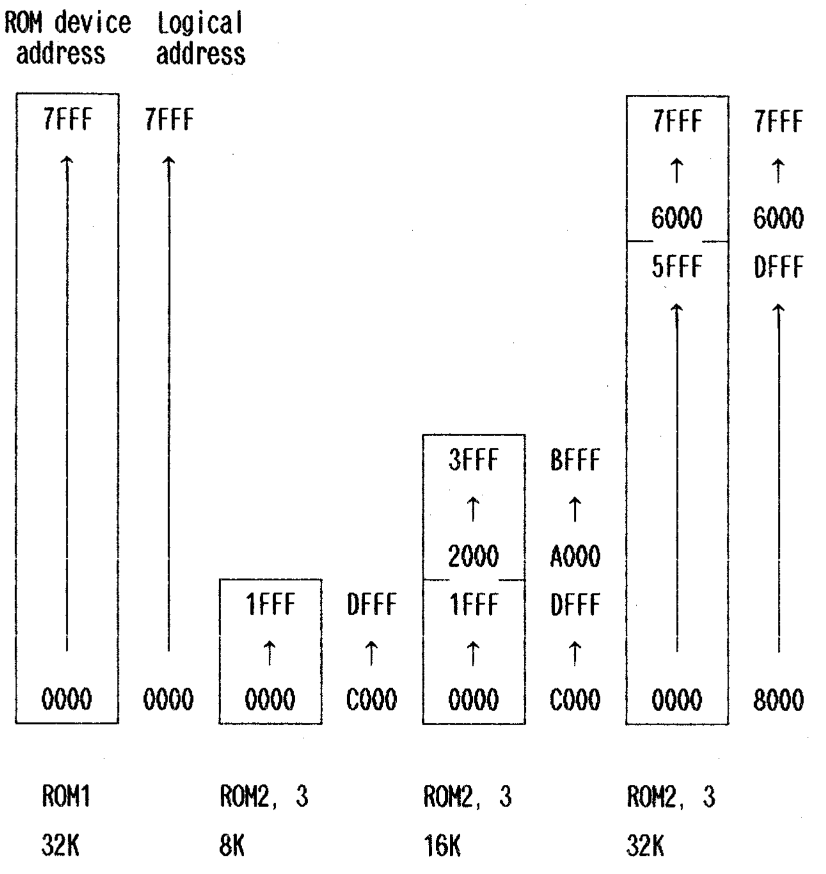



Fig. 1.2.1 PINE Memory Map

Note: Note the relationship between the logical and physical ROM addresses when programming ROM devices.




* See also the figure on the previous page.

## 1.3 I/O Map

### 1.3.1 Introduction

The PINE I/O addresses space is allocated to the three gate array LSIs (i.e., GAPNIT, GAPNDL, and GPNIO) and the I/O devices in the external expansion box. The GAPNIT are assigned I/O addresses PØØH through PØ7H, the GAPNDL is assigned PØ8H through PØFH, the GAPNIO is assigned P1ØH through P1FH, and the external I/O devices P2ØH through PFFH.

### 1.3.2 I/O Address Space

Table 1.3.1 lists the I/O addresses assigned to the PINE. In the table, I/O address bits identified by an asterisk (EDJ and ECA) are used only for development boards and valid only for board development. The unused I/O addresses between PØØH through P1FH must not be used by the user. Any accesses to inhibited I/O address may cause computer malfunctions.

Details about the I/O registers are found in Chapter 2, "I/O Registers."

| I/O Adderss | Read (bit) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Write (bit) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Device |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | ICRL・C ICR・Low command trigger (8) | | | | | | | | CTLR1 control register 1 (8) | | | | | | | | GAPNIT |
| | 8 bits data | | | | | | | | BRG3 | BRG2 | BRG1 | BRG0 | SWBCR | BCR1 | BCR0 | SLBCR | |
| 01 | ICRH・C ICR・High command trigger (8) | | | | | | | | CMDR command register (3) | | | | | | | | |
| | 8 bits data | | | | | | | | | | | | | RESET OVF | RESET RDYSIO | SET RDYSIO | |
| 02 | ICRL・B ICR・Low barcode trigger (8) | | | | | | | | CTLR2 control register (2) | | | | | | | | |
| | 8 bits data | | | | | | | | | | | | | | RMT | MIC | |
| 03 | ICRH・B ICR・High barcode trigger (8) | | | | | | | | | | | | | | | | |
| | 8 bits data | | | | | | | | | | | | | | | | |
| 04 | ISR interrupt status register (5) | | | | | | | | IER interrupt enable register (5) | | | | | | | | |
| | | | | EXT | OVF | ICF | RxRDY | 7508 | | | | EXT | OVF | ICF | RxRDY | 7508 | |
| 05 | STR status register (8) | | | | | | | | BANKR bank register (8) | | | | | | | | |
| | BANK3 | BANK2 | BANK1 | BANK0 | RDYSIO | RDY | BCRD | EAR | BANK3 | BANK2 | BANK1 | BANK0 | *EDU | *ECA | CKSW1 | CKSW0 | |
| 06 | SIOR serial IO register (8) | | | | | | | | SIOR serial IO register (8) | | | | | | | | |
| | 8 bits data | | | | | | | | 8 bits data | | | | | | | | |
| 07 | | | | | | | | | | | | | | | | | |
| 08 | | | | | | | | | VADR VRAM start address register (5) | | | | | | | | GAPNDI |
| | | | | | | | | | A15 | A14 | A13 | A12 | A11 | | | | |
| 09 | | | | | | | | | YOFF Y offset register (7) | | | | | | | | |
| | | | | | | | | | DSP | | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | |
| 0A | | | | | | | | | FR frame register (4) | | | | | | | | |
| | | | | | | | | | | | | | F3 | F2 | F1 | F0 | |

1. 3. 1 (1)

| I/O Adderss | Read (bit) 7 6 5 4 3 2 1 0 | Write (bit) 7 6 5 4 3 2 1 0 | Device |
|---|---|---|---|
| 0B | | SPUR speed-up register (6)<br>— \| PRE2 \| PRE1 \| PRE0 \| — \| POST2 \| POST1 \| POST0 | GAPNDL |
| 0C | | | GAPNDL |
| 0D | | | GAPNDL |
| 0E | | | GAPNDL |
| 0F | | | GAPNDL |
| 10 | CTG IF (cartridge interface) address space | CTG IF (cartridge interface) address space | GAPNIO |
| 11 | CTG IF (cartridge interface) address space | CTG IF (cartridge interface) address space | GAPNIO |
| 12 | CTG IF (cartridge interface) address space | CTG IF (cartridge interface) address space | GAPNIO |
| 13 | CTG IF (cartridge interface) address space | CTG IF (cartridge interface) address space | GAPNIO |
| 14 | ARTDIR ART data input register (8)<br>7/8 bits data | ARTDOR ART data output register (8)<br>7/8 bits data | GAPNIO |
| 15 | ARTSR ART status register (7)<br>RDSR \| — \| FE \| OE \| PE \| Tx empty \| Rx RDY \| Tx RDY | ARTMR ART mode register (4)<br>STOP \| — \| EVEN \| PEN \| — \| DATA \| — \| — | GAPNIO |

1.3.1 (2)

| I/O Adderss | Read 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (bit) | Write 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (bit) | Device |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 16 | IOSTR IO status register (8) | | | | | | | | ARTCR ART command register (6) | | | | | | | | GAPNIO |
| | CAUD | CSEL | RCTS | RCD | RXD | SIN | PERR | PBSY | | | RRTS | ER | SBRK | RxE | RDTR | TxE | |
| 17 | | | | | | | | | PDR printer data register (8) | | | | | | | | |
| | | | | | | | | | 8 bits data | | | | | | | | |
| 18 | | | | | | | | | SWR switch register (5) | | | | | | | | |
| | | | | | | | | | | | | AUSW | SSW1 | SSW0 | CSW1 | CSN0 | |
| 19 | | | | | | | | | IOCTLR IO control register (8) | | | | | | | | |
| | | | | | | | | | SP | LED2 | LED1 | LED0 | $\overline{CRS}$ | SOUT | $\overline{PINI}$ | PSTB | |
| 1A | | | | | | | | | | | | | | | | | |
| 1B | | | | | | | | | | | | | | | | | |
| 1C | | | | | | | | | | | | | | | | | |
| 1D | | | | | | | | | | | | | | | | | |
| 1E | | | | | | | | | | | | | | | | | |
| 1F | | | | | | | | | | | | | | | | | |
| 20 ~ FF | Reserved for the I/O devices in the external expansion box. | | | | | | | | | | | | | | | | |

1.3.1 (3)

## 1.4 Miscellaneous

### 1.4.1 Z-8Ø Wait Operation

The PINE uses part of the DRAM address space as a video RAM area. Since the M1 cycle is too short to successfully access the VRAM area, the PINE Z-8Ø CPU inserts one wait state into every M1 cycle. This means that one wait state is inserted into every M1 cycle while an application program is being executed in DRAM. No wait state is insert when a program on ROM is executed and no DRAM is accessed. It follows from this discussion that the same program executes at different execution speeds when it is executed in DRAM and when it is implemented on ROM.

## CHAPTER 2 I/O REGISTERS

# CHAPTER 2 I/O REGISTERS

This chapter describes the I/O registers, their usage, and their relationship to the PINE operating system.

## 2.1 General

The PINE I/O registers are located in I/O port addresses PØØH through PFFH. I/O addresses PØØH through P1FH are for the internal I/O devices and P2ØH through PFFH for the external I/O devices.

The optional external RAM disk unit uses I/O addresses P9ØH through P94H. I/O address P94H is used in the read mode to check the presence or absence of the external RAM disk so it is not available to the user when an external device is used (through the system bus).

Since the output state of some I/O registers is maintained by the operating system, the user program must rewrite the corresponding system RAM areas when rewriting such I/O registers. (See Section 2.3, "Programming Considerations").

## 2.2 I/O Register Descriptions

### 2.2.1 PØØH: ICRL.C (Input Capture Register Low Command Trigger) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | ICR 7 | Input capture register lower order 8 bits |
| 6 | ICR 6 | |
| 5 | ICR 5 | |
| 4 | ICR 4 | |
| 3 | ICR 3 | |
| 2 | ICR 2 | |
| 1 | ICR 1 | |
| 0 | ICR 0 | |

Explanation:
PØØH is assigned to the lower 8 bits of the input capture register. The contents (both higher and lower order bytes) of the FRC (Free Running Counter) are latched into the ICR (Input Capture Register) immediately when this register is read. The higher order value can be obtained by reading I/O address PØ1H (ICRHC).

PØØH is used to read the contents of the FRC.

2.2.2 PØØH: CTLR1 (Control Register 1) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | BRG 3 | Band Rate Generator Select |
| 6 | BRG 2 | |
| 5 | BRG 1 | |
| 4 | BRG 0 | |
| 3 | SWBCR | Power switch for +5vdc power to the barcode reader<br>=1 : Power on<br>=0 : Power off |
| 2 | BCR1 (up) | Barcode mode select |
| 1 | BCR0(down) | |
| 0 | SLBCR | Selects the trigger signal for latching the FRC data into the FRC.<br>=1 : Barcode reader input<br>=0 : External cassette ear input |

Explanation:
BRG3-BRGØ specify the baud rate for the serial interface and BCR1 and BCR2 specify the polarity of the ICR trigger.

Band Rate Generator Select

| B R G | | | | Transmit | | Receive | |
|---|---|---|---|---|---|---|---|
| 3 | 2 | 1 | 0 | T×C | Baud rate | R×C | Baud rate |
| 0 | 0 | 0 | 0 | 1.74545 k | 110 | 1.74545 k | 110 |
| 0 | 0 | 0 | 1 | 2.4 k | 150 | 2.4 k | 150 |
| 0 | 0 | 1 | 0 | 4.8 k | 300 | 4.8 k | 300 |
| 0 | 0 | 1 | 1 | 9.6 k | 600 | 9.6 k | 600 |
| 0 | 1 | 0 | 0 | 19.2 k | 1.2 k | 19.2 k | 1.2 k |
| 0 | 1 | 0 | 1 | 38.4 k | 2.4 k | 38.4. k | 2.4 k |
| 0 | 1 | 1 | 0 | 76.8 k | 4.8 k | 76.8 k | 4.8 k |
| 0 | 1 | 1 | 1 | 153.6 k | 9.6 k | 153.6 k | 9.6 k |
| 1 | 0 | 0 | 0 | 19.2 k | 1.2 k | 1.2 k | 75 |
| 1 | 0 | 0 | 1 | 1.2 k | 75 | 19.2 k | 1.2 k |
| 1 | 0 | 1 | 0 | 307.2 k | 19.2 k | 307.2 k | 19.2 k |
| 1 | 0 | 1 | 1 | 614.4 k | 38.4 k | 614.4 k | 38.4 k |
| 1 | 1 | 0 | 0 | 3.2 k | 200 | 3.2 k | 200 |

Barcode mode select settings

| BCR1 | BCR0 | Trigger polarity |
|---|---|---|
| 0 | 0 | Trigger inhibit |
| 0 | 1 | Falling-edge trigger |
| 0 | 1 | Rising-edge trigger |
| 0 | 1 | Rising-/falling-edge trigger |

Programming note:
The PINE OS stores the write data to the CTLR1 in system RAM area RZCTLR1 (ØFØØ1H) for use during update processing.
When writing the CTLR1 directly from a user program, therefore, it is necessary to rewrite the contents of the RZCTLR1 simultaneously. The bit format of the RZCTLR1 is identical to that of the CTLR1.
Example: Turning on barcode power

```
        LD    A, (RZCTLR1)
        OR    Ø8H
        LD    (RZCTLR1), A
        OUT   (CTLR1), A
```

The OS also updates the baud rate setting through BIOS RSIOX or during accesses to the FDD.

2.2.3 PØ1H: ICRH.C (Input Capture Register High Command Trigger) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | ICR 15 | Input capture register higher order 8 bits |
| 6 | ICR 14 | |
| 5 | ICR 13 | |
| 4 | ICR 12 | |
| 3 | ICR 11 | |
| 2 | ICR 10 | |
| 1 | ICR 9 | |
| 0 | ICR 8 | |

Explanation:
PØ1H is read to fetch the contents of the FRC. Bits ICR15-ICR8 are latched immediately when the ICRLC (PØØH) is read. Accordingly, the ICRLC must be read before the ICRHC is read.

### 2.2.4 PØ1H: CMDR (Command Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | | |
| 5 | | |
| 4 | | |
| 3 | | |
| 2 | RES OVF | =1 : Resets the INTR signal set by an FRC overflow interrupt.<br>=0: Does nothing. |
| 1 | RES RDYSIO | =1 : Resets the RDYSIO signal (indicating the 75Ø8 ready state).<br>=0 : Does nothing. |
| 0 | SET RDYSIO | =1 : Sets the RDYSIO signal used for communication with the 75Ø8.<br>=0 : Does nothing.<br><br>This bit is used only the system. |

Programming note:
The PINE OS uses the RES OVF bit during OVF interrupt processing and the RES RDYSIO bit during communication with the 75Ø8.

### 2.2.5 PØ2H: ICRL.B (Input Capture Register Low Barcode Trigger) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | ICR 7 | Input capture register lower order 8 bits set by the state transition of the barcode or external cassette signal. |
| 6 | ICR 6 | |
| 5 | ICR 5 | |
| 4 | ICR 4 | |
| 3 | ICR 3 | |
| 2 | ICR 2 | |
| 1 | ICR 1 | |
| 0 | ICR 0 | |

Explanation:
PØ2H is assigned to the lower 8 bits of the ICR which are loaded with data from the FRC on the negative-to-positive or positive-to-negative transition of the barcode (BCRD) or external cassette (EAR) signal. The transition of the BCRD or EAR signal is identified by the INT2 signal (ICF) being made active. Either barcode reader or external cassette is selected by the CTLR1, bit SWBCR.

2.2.6 PØ2H: CTLR2 (Control Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | | |
| 5 | | |
| 4 | | |
| 3 | | |
| 2 | | |
| 1 | RMT | Turns on or off the external cassette remote mode.ready state).<br>=1 :Turns on remote mode.<br>=0 :Turns off remote mode. |
| 0 | MIC | Write signal (MIC output) to the external cassettedrive. |

Explanation:
PØ2H is used to control the RMT and MIC lines of the external cassette interface.

Programming note:
The PINE OS does not support the external cassette. It is supported only by BASIC.

2.2.7 PØ3H: ICRH.B (Input Capture Register High Barcode Trigger) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | ICR 15 | Input capture register higher order 8 bits set by the state transition of the barcode or external cassette signal. |
| 6 | ICR 14 | |
| 5 | ICR 13 | |
| 4 | ICR 12 | |
| 3 | ICR 11 | |
| 2 | ICR 10 | |
| 1 | ICR 9 | |
| 0 | ICR 8 | |

Explanation:
PØ2H is assigned to the higher 8 bits of the ICR which are loaded with data from the FRC on the negative-to-positive or positive-to-negative transition of the barcode (BCRD) or external cassette (EAR) signal. Reading this register resets the INT2 signal (ICF) that is made active by the transition of the BCRD or EAR.

2.2.8 PØ4H: ISR (Interrupt Status Register) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Always set to Ø. |
| 6 | | |
| 5 | | |
| 4 | INT4(EXT) | External interrupt signal. Reset by returning a response signal to the external expansion box. |
| 3 | INT3 (OVF) | Interrupt signal set when an FRC overflow condition occurs. Reset by setting the CMDR (PØ1H) RES OVF bit to 1. |
| 2 | INT2 (ICF) | Interrupt signal set immediately when the the FRC data is latched into the ICR on the state transition of the barcode (BCRD) or external cassette (EAR) signal. This interrupt does not occur when latching is inhibited. This bit is reset by reading ICRH.B (at PØ3H). |
| 1 | INT1 (ART) | Interrupt signal set when the ART RxRDY signal is set to 1. Reset by reading ARTDIR (P14H). |
| 0 | INT0 (7508) | Interrupt signal generated by the 75Ø8 slave CPU. Reset by giving a response to the 75Ø8. |

Explanation:
INT4 through INTØ can be read even if the corresponding interrupts are masked off. INTØ is given the highest priority and INT4 the lowest priority.

Programming note:
The PINE OS uses 75Ø8, ART, and OVF interrupts.

2.2.9 PØ4H: IER (Interrupt Enable Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7<br>6<br>5 | | Ignored |
| 4 | IER 4 | INT4 (EXT) interrupt status.<br>1 : Enable 0 : Disable |
| 3 | IER 3 | INT3 (OVF) interrupt status.<br>1 : Enable 0 : Disable |
| 2 | IER 2 | INT2 (ICF) interrupt status.<br>1 : Enable 0 : Disable |
| 1 | IER 1 | INT1 (ART) interrupt status.<br>1 : Enable 0 : Disable |
| 0 | IER 0 | INTØ (75Ø8) interrupt status.<br>1 : Enable 0 : Disable |

Explanation:
The IER bits indicate the interrupt status of the corresponding interrupts.

Programming note:
The PINE OS stores the write data to the IER in system RAM area RZIER (ØF53EH) for use during update processing.
When writing the IER directly from a user program, therefore, it is necessary to rewrite the contents of the RZIER simultaneously.
The bit format of the RZIER is identical to that of the IER.

Example: Enabling EXT interrupts

```
        DI
        LD    A, (RZIER)          RZIER:(ØF53EH)
        OR    1ØH                 IER: (Ø4H)
        LD    (RZIER),A
        OUT   (IER),A
        EI
```

The PINE OS turns on and off the interrupt mask using BIOS MASKI.

In the normal state, 75Ø8 and OVF interrupts are enabled and ART interrupt is enabled when the BIOS RSIOX open function is executed and disabled when the BIOS RSIOX close function is executed. ICF and EXT interrupts are disabled.

2.2.10 PØ5H: STR (Status Register) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | BANK 3 | Main Memory Bank Register |
| 6 | BANK 2 | |
| 5 | BANK 1 | |
| 4 | BANK 0 | |
| 3 | RDYSIO | Controls the serial bus used to interface to the 75Ø8 slave CPU.<br>=1 : Enables access to the 75Ø8.<br>=0 : Disables access to the 75Ø8. |
| 2 | RDY | RDY signal from the 75Ø8.<br>Normally not used. |
| 1 | BCRD | Data input from the barcode reader. |
| 0 | EAR | Data input from the external cassette. |

Explanation:
See Section 1.2, "Address Map" for the values of BANK3 through BANKØ.

2.2.11 PØ5H: BANKR (Bank Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | BANK 3 | Main Memory Bank Register |
| 6 | BANK 2 | |
| 5 | BANK 1 | |
| 4 | BANK 0 | |
| 3 | EDU | Development board enable signal.<br>1: Uses the RAM on the development board.<br>Ø: Does not use the RAM on the development board.<br>Normally set to Ø. |
| 2 | ECA | RAM select signal for the development board.<br>Normally set to Ø. |
| 1 | CKSW 1 | Clock Switch |
| 0 | CKSW 0 | |

Explanation:
See Section 1.2, "Address Map" for the values of BANK3 through BANKØ.

Programming note:
The PINE OS stores the write data to the BANKR in system RAM area RZBANKR (ØF53DH) for use during update processing.
When writing the BANKR directly from a user program, therefore, it is necessary to rewrite the contents of the RZBANKR simultaneously.
The bit format of the RZBANKR is identical to that of the BANKR.

Clock Switch

| CKSW1 | CKSW0 | System clock |
|---|---|---|
| 1 | 0 | 3. 6864 MHZ |
| 1 | 1 | 3. 072 MHZ |
| 0 | * | 3. 4576 MHZ |

* : Ignored

Note: For the PINE, CKSW1 must be set to 1 and CKSW0 to 0 because the PINE uses the 3.6864 MHz system clock. Setting these bits to other values may cause serial I/F or timer malfunctions.

The PINE OS provides LOADX, STORX, LDIRX, JUMPX, and CALLX as BIOS functions for controlling the banks. For details of these routines, see 4.4, "Bank Switching" in Part II.

2.2.12 P06H: SIOR (Serial I/O Register) (read/write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | SIO 7 | 7508 data register |
| 6 | SIO 6 | |
| 5 | SIO 5 | |
| 4 | SIO 4 | |
| 3 | SIO 3 | |
| 2 | SIO 2 | |
| 1 | SIO 1 | |
| 0 | SIO 0 | |

Explanation:
P06H holds 8-bit data received from the 7508 in the read mode and 8-bit data to be sent to the 7508 in the write mode.

2.2.13 PØ8H: VADR (VRAM Start Address Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | A15 | V-RAM Start Address |
| 6 | A14 | |
| 5 | A13 | |
| 4 | A12 | |
| 3 | A11 | |
| 2 | | Ignored |
| 1 | | |
| 0 | | |

Explanation:
The VADR addresses the VRAM area. It generates the five highest order address bits, providing a VRAM address space of (A15 A14 A13 A12 A11 Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø) to (A15 A14 A13 A12 A11 1 1 1 1 1 1 1 1 1 1 1). This allows the VRAM area to be located on any 2K-byte boundary.

Programming note:
The PINE OS allocates addresses ØD8ØØH through ØDFFFH for the system screen VRAM (VRAM2) and addresses ØEØØØH through ØE7FFH for the user screen VRAM (VRAM1).

The address of the currently active VRAM is stored in LSCRVRAM (ØF294H). The VADR is loaded with the address data from LSCRVRAM + 1 (F295H).

2.2.14 PØ9H: YOFF (Y Offset Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | DSP | Turns on and off LCD display.<br>=1 : Turns on display.<br>=0 : Turns off display. |
| 6 | | Ignored |
| 5 | Y5 | Y-direction offset register (YOFF) |
| 4 | Y4 | |
| 3 | Y3 | |
| 2 | Y2 | |
| 1 | Y1 | |
| 0 | Y0 | |

Explanation:
The YOFF defines the correspondence between the VRAM and the LCD panel. It gives the offset with respect to the top of the VRAM at which display is to start. When display reaches the bottom of the VRAM, it wraps around to the top of the VRAM. One screenful of display ends at (YOFF - 1)th dot line.

Programming note:
The PINE OS uses the YOFF for vertical scrolling. The current value of the YOFF is saved in LVRAMYOFF (ØF2AØH).

2.2.15 P0AH: FR (Frame Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | | |
| 5 | | |
| 4 | | |
| 3 | FR3 | Frame Register |
| 2 | FR2 | |
| 1 | FR1 | |
| 0 | FR0 | |

Explanation:
The FR defines the LCD frame frequency. The table below shows the relationship between the frame register and frame frequencies.

| FR | | | | LCD frame frequency (in Hz) | | |
|---|---|---|---|---|---|---|
| FR3 | FR2 | FR1 | FR0 | 3.68MHz | 3.07MHz | 2.45MHz |
| 0 | 1 | 0 | 0 | 106 | 88 | 70 |
| 0 | 1 | 0 | 1 | 86 | 72 | 57 |
| 0 | 1 | 1 | 0 | 72 | 60 | 48 |
| 0 | 1 | 1 | 1 | 62 | 52 | 41 |
| 1 | 0 | 0 | 0 | 55 | 46 | 36 |
| 1 | 0 | 0 | 1 | 49 | 41 | 32 |
| 1 | 0 | 1 | 0 | 44 | 37 | 29 |
| 1 | 0 | 1 | 1 | 40 | 33 | Invalid |
| 1 | 1 | 0 | 0 | 37 | Invalid | Invalid |
| 1 | 1 | 0 | 1 | 34 | Invalid | Invalid |

FR values (0000) through (0011), (1110), and (1111) are invalid.

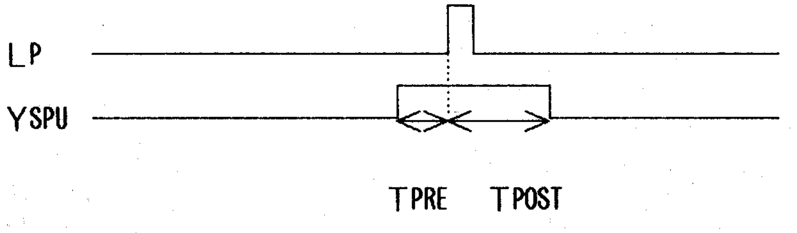
Programming note:
The 3.68 MHz column in the table applies to the PINE since its system clock is 3.6864 MHz. The PINE OS loads the FR with 06H when executing the power-on, reset, and system initialize functions.

2.2.16 PØBH: SPUR (SpeedUp Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | PRE2 | Define TPRE. |
| 5 | PRE1 | |
| 4 | PRE0 | |
| 3 | | Ignored |
| 2 | POST2 | Define TPOST. |
| 1 | POST1 | |
| 0 | POST0 | |

Explanation:
The SPUR defines the timing at which the impedance of the power supply to the LCD is to be reduced to suppress the voltage fluctuations occurring (due to increased current) during the rewrite of LCD panel data.

TPRE and TPOST define the pulse width of the YSPU which is used to save the power to the LCD unit. TPRE specifies the time interval before the LP signal and TPOST the delay time after LP. LP an LCD control signal and gives the latch pulse to the LCD shift register.




The table below lists the TPRE and TPOST values for the frame frequency of 5Ø. The actual time values can be obtained from:

$$\text{TPRE (TPOST)} = \frac{5Ø}{\text{Frame frequency}} \times \text{(Value taken from table)}$$

| PRE2 | PRE1 | PRE0 | TPRE (μs) |
|---|---|---|---|
| 0 | 0 | 0 | 77 |
| 0 | 0 | 1 | 67 |
| 0 | 1 | 0 | 57 |
| 0 | 1 | 1 | 48 |
| 1 | 0 | 0 | 38 |
| 1 | 0 | 1 | 28 |
| 1 | 1 | 0 | 18 |
| 1 | 1 | 1 | 9.2 |

| POST2 | POST1 | POST0 | T POST (μs) |
|---|---|---|---|
| 0 | 0 | 0 | 0.2 |
| 0 | 0 | 1 | 9.9 |
| 0 | 1 | 0 | 19 |
| 0 | 1 | 1 | 29 |
| 1 | 0 | 0 | 39 |
| 1 | 0 | 1 | 48 |
| 1 | 1 | 0 | 58 |
| 1 | 1 | 1 | 68 |

Programming note:
The PINE OS loads the SPUR with 43H when executing the power-on, reset, and system initialize functions.

2.2.17 P1ØH - P13H

Explanation
P1ØH through P13H are reserved for the cartridge interface. Their assignments differ depending on the cartridge mode (HS, DB, IO, or OT mode). See Section 4.1, "Cartridge Interface" for details about P1ØH through P13H.

2.2.18 P14H: ARTDIR (ART Data Input Register) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | RD7 | Receive data. |
| 6 | RD6 | |
| 5 | RD5 | |
| 4 | RD4 | |
| 3 | RD3 | |
| 2 | RD2 | |
| 1 | RD1 | |
| 0 | RD0 | |

Explanation:
P14H is loaded with the parallel data converted from the serial data received over the RxD line. Bit 7 (RD7) is set to Ø when the 7-bit data format is used.

Programming note:
In PINE OS, serial data reception is conducted by an interrupt processing routine and the transfer of received data to the application program is done by a BIOS RSIOX function.

2.2.19 P14H: ARTDOR (ART Data Output Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | TD7 | Send data. |
| 6 | TD6 | |
| 5 | TD5 | |
| 4 | TD4 | |
| 3 | TD3 | |
| 2 | TD2 | |
| 1 | TD1 | |
| 0 | TD0 | |

Explanation:
P14H is loaded with the parallel data to be sent over the serial TxD line. Bit 7 (TD7) is ignored when the 7-bit data format is used.

Programming note:
In PINE OS, serial data transmission and interface to the application program are conducted by BIOS RSIOX functions.

2.2.2Ø P15H: ARTSR (ART Status Register) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | RDSR | Data Set Ready signal. Set to 1 when the RS-232C interface DSR terminal is set active. |
| 6 | | Always set to Ø. |
| 5 | FE | Set to 1 to indicate a framing error. |
| 4 | OE | Set to 1 to indicate an overrun error. |
| 3 | PE | Set to 1 to indicate a parity error. |
| 2 | Tx Empty | Indicates that no data is present in the transmitter block. This bit is set when the ARTDOR transmit buffer and the parallel-to-serial converter are both empty. |
| 1 | Rx RDY | When set to 1, generates an INT1 (ART) interrupt request to the Z-8Ø CPU to indicate that a data byte is received from the serial communication line. RxRDY is reset by reading the ARTDIR receive buffer (P14H). This bit may also be reset by the reset input or error reset command. |
| 0 | Tx RDY | Set to 1 when the ARTDOR output buffer is emptied and reset when the buffer is loaded with send data. |

Explanation:

FE (bit 5): The receive data processing is not affected when a framing error condition occurs. The PINE continues to receive the next data byte and checks it against the framing error condition. If the stop bits are received normally, the PINE resets the FE bit.

OE (bit 4): The receive data processing continues even when an overrun error occurs. The OE, however, is not reset when the next data byte is received normally. The OE bit can be reset only by issuing the error reset command (ER = 1) or reset signal.

PE (bit 3): The resetting conditions for the PE bit are identical to those for the FE bit. Parity is checked only when PEN is set to 1, that is, PE is held at Ø when PEN is Ø.

2.2.21 P15H: ARTMR (ART Mode Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | STOP | Specifies the number of stop bits.<br>=1 : 2bit<br>=0 : 1bit |
| 6 | | Ignored |
| 5 | EVEN | Specifies the parity check mode (valid only when PEN is 1).<br>=1 : Even parity<br>=0 : Odd parity |
| 4 | PEN | Enables or disables parity checking.<br>=1 : Enables parity checking.<br>=0 : Disables parity checking. |
| 3 | | Ignored |
| 2 | DATA | Specifies the length of the serial data.<br>=1 : 8bit<br>=0 : 7bit |
| 1 | | Ignored |
| 0 | | |

Programming note:
The PINE OS stores the ARTMR data in RZARTMR (ØFØØ3H) in the system RAM area for use during update processing. When writing the ARTMR directly from a user program, therefore, it is necessary to rewrite the contents of the RZARTMR simultaneously. The bit format of the RZARTMR is identical to that of the ARTMR.

Writing data to the ARTMR is supported by a BIOS RSIOX function.

2.2.22 P16H: IOSTR (IO Status Register) (read mode)

| Bit | Name | Description |
|---|---|---|
| 7 | CAUD | Audio input signal from the cartridge connector (has nothing to do with AUSW). |
| 6 | CSEL | Cartridge option select signal.<br>=0 : HS (Hand Shake) mode<br>=1 : Other modes |
| 5 | RCTS | RS-232C CTS signal.<br>Set to 1 when RS-232C CTS is set active. |
| 4 | RCD | RS-232C CD signal.<br>Set to 1 when RS-232C CD is set active. |
| 3 | RXD | Serial data input. |
| 2 | SIN | Status signal from the SIO interface. |
| 1 | PERR | Error signal from the Centronics interface (A 1 in this bit indicates a printer error condition). |
| 0 | PBUSY | Busy signal from the Centronics interface (A 1 in this bit indicates a printer busy condition). |

Explanation:
The state of the ART inputs (RDSR, RCTS, RCD, etc.) is determined as follows:

| | |
|---|---|
| 2.6 volts and up: | High (active) |
| Ø.7 to 2.6 volts: | Unpredictable |
| Ø.7 volts and below: | Low (inactive) |

2.2.23 P16H: ARTCR (ART Command Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | | |
| 5 | RRTS | RS-232C RTS signal. Setting the RRTS bit to 1 sets the RTS pin in the RS-232C interface active. |
| 4 | ER | Resets the OE, FE, and PE bits. ER must be set to 1 when RXE is set to 1. Setting ER to 1 generates a pulse (only during the write operation) so it need not be reset. |
| 3 | SBRK | Break output. Setting this bit to 1 forces the TXD line to Ø (valid only when TXE is 1). |
| 2 | RXE | Enables or disables serial reception.<br>=1 : Enable<br>=0 : Disable |
| 1 | RDTR | RS-232C DTR signal. Setting this bit to 1 sets the DTR pin in the RS-232C interface active. |
| 0 | TXE | Enables or disables serial transmission.<br>=1 : Enable<br>=0 : Disable<br>TXD is held in the 1 (mark) level while TXE is Ø. |

Programming note:
The PINE OS stores the ARTCR data in RZARTCR (ØFØØ4H) in the system RAM area for use during update processing. When writing the ARTCR directly from a user program, therefore, it is necessary to rewrite the contents of the RZARTCR simultaneously. The bit format of the RZARTCR is identical to that of the ARTCR.

Writing data to the ARTCR is supported by a BIOS RSIOX function.

### 2.2.24 P17H: PDR (Printer Data Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | PDR7 | Print data to the Centronics interface |
| 6 | PDR6 | |
| 5 | PDR5 | |
| 4 | PDR4 | |
| 3 | PDR3 | |
| 2 | PDR2 | |
| 1 | PDR1 | |
| 0 | PDR0 | |

Explanation:
See Section 4.4, "Other Interfaces" for the method of transferring print data to the Centronics interface.

Programming note:
Writing data to the Centronics interface is supported by the BIOS LIST function.

### 2.2.25 P18H: SWR (Switch Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | | Ignored |
| 6 | | |
| 5 | | |
| 4 | AUSW | Used to mask on or off the CAUD input from the cartridge.<br>=0 : Masks off CAUD.<br>=1 : Masks on CAUD. |
| 3 | SSW1 | Serial mode |
| 2 | SSW0 | |
| 1 | CSW1 | Cartridge I/F mode |
| 0 | CSW0 | |

Explanation:
P18H is used to define the mode of the serial and cartridge interfaces.

Serial mode

| SSW1 | SSW0 | RXD | TXD |
|---|---|---|---|
| 0 | 0 | Cartridge SIO | Cartridge SIO |
| 0 | 1 | SIO | SIO |
| 1 | 0 | RS-232C | RS-232C |
| 1 | 1 | RS-232C | SIO |

Cartridge mode

| CSW1 | CSW0 | Mode |
|---|---|---|
| 0 | 0 | HS (HandShake mode) |
| 0 | 1 | IO (Input/Output) mode |
| 1 | 0 | DB (Data Bus) mode |
| 1 | 1 | OT (Output port) mode |

Programming note:
The PINE OS stores the SWR data in RZSWR (ØFØØ5H) in the system RAM area for use during update processing. When writing the SWR directly from a user program, therefore, it is necessary to rewrite the contents of the RZSWR simultaneously. The bit format of the RZSWR is identical to that of the SWR.

Example: Switching the cartridge mode to the IO mode

```
        LD    A, (RZSWR)              RZSWR: (ØFØØ5H)
        AND   ØFCH                    SWR: (18H)
        OR    Ø1H
        LD    (RZSWR),A
        OUT   (SWR), A
```

Switching the serial mode can be accomplished using a BIOS RSIOX function.

2.2.26 P19H: IOCTLR (IO Control Register) (write mode)

| Bit | Name | Description |
|---|---|---|
| 7 | SP | Output to the loudspeaker. SP must be set to Ø when the CAUD output is to be directed to the loudspeaker. Set AUSW to Ø when directing the SP output to the loudspeaker. |
| 6 | LED2 | LED output port |
| 5 | LED1 | LED output port |
| 4 | LED0 | LED output port |
| 3 | $\overline{CRS}$ | Cartridge reset signal used to software through reset the cartridge. Setting this bit to Ø resets the cartridge. |
| 2 | $\overline{SOUT}$ | Control signal to the SIO interface. |
| 1 | $\overline{PINT}$ | Initial output to the Centronics interface. Setting this bit to Ø initializes the printer. |
| 0 | PSTB | Strobe signal to the Centronics interface.<br>=0 : Normal<br>=1 : Data strobe |

Programming note:
The PINE OS stores the IOCTLR data in RZIOCTLR (ØFØØ6H) in the system RAM area for use during update processing. When writing the IOCTLR directly from a user program, therefore, it is necessary to rewrite the contents of the RZIOCTLR simultaneously. The bit format of the RZIOCTLR is identical to that of the IOCTLR.

In the PINE OS, SP is referenced by the BIOS BEEP function and LED2 through LEDØ by the BIOS input functions. LED2 through LEDØ is controlled by the CONOUT function (ESC + (AØH to A5H)).

2.2.27 P2ØH-PFFH (read/write mode)

P2ØH through PFFH are used for external RAM disk drives and other optional units.

Although I/O addresses P2ØH through PFFH are always available if the system bus is used, the PINE OS examines I/O address P94H to determine whether an external RAM disk unit is connected to the system bus. This address is reserved only for the external RAM disk unit. Under the PINE OS, a 1 in bit 7 of P94H indicates that an external RAM disk unit is attached.

## 2.3 Programming Considerations

### 2.3.1 Initial I/O Register Reset

To save gate count, the outputs of some control registers in the PINE gate array LSIs are set to Ø by a special means immediately after a initial reset.
When an initial reset occurs, the outputs of control registers are masked to the Ø level by the register output control flip-flop (see Figure 2.3.1) even if their contents are unpredictable. After the CPU is started, the initial program initializes the registers and remove the register mask. Externally, the registers are given the appearance of being reset. This resetting method is called pseudo-reset.

The PINE registers are divided into three groups according to the way they are initialized:

1) Registers that are reset in the pseudo-reset mode.
2) Registers that are reset in the normal mode.
3) Registers that are not reset at all.

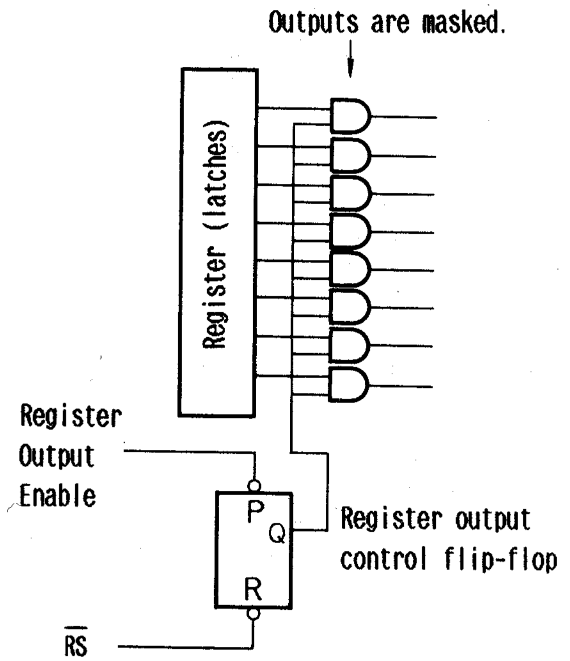



Fig. 2.3.1 Resetting a Register in Pseudo-reset mode

### 2.3.1.1 Registers that are reset in pseudo-reset mode

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CTLR1 (P00H) | | | | | SWBCR | BCR1 | BCR0 | |
| IER (P04H) | | | | EXT | OVF | ICF | RxRDY | 7508 |
| BANKR (P05H) | BANK3 | BANK2 | BANK1 | BANK0 | | | | |

Registers CTLR1 (PØØH), IER (PØ4H), and BANKR (PØ5H) are reset in the pseudo-reset mode by a single output control flip-flop. Their masks are removed by writing the CTLR1 register (PØØH).

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ARTMR (P15H) | STOP | | EVEN | PEN | | DATA | | |
| ARTCR (P16H) | | | RRTS | ER | SBRK | RXE | RDTR | TXE |
| SWR (P18H) | | | | AUSW | SSW1 | SSW0 | CSW1 | CSW0 |
| IOCTLR(P19H) | SP | LED2 | LED1 | LED0 | $\overline{\text{CRS}}$ | SOUT | $\overline{\text{PINT}}$ | PSTB |

Registers ARTMR (P15H), ARTCR (P16H), SWR (P18H), and IOCTLR (P19H) are reset in the pseudo-reset mode by a single output control flip-flop. Their masks are removed by writing the ARTMR register (P15H).

### 2.3.1.2 Registers that are reset in normal mode

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CTLR2 (P02H) | | | | | | | RMT | MIC |
| YOFF (P09H) | DSP | | | | | | | |

2.3.1.3 Registers that are not reset

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CTLR 1 (P00H) | BRG3 | BRG2 | BRG1 | BRG0 | | | | SLBCR |
| BANKR (P05H) | | | | | | | CKSW1 | CKSW0 |
| SIOR (P06H) | Transmit Data to 4 bit CPU | | | | | | | |
| VADR (P08H) | A15 | A14 | A13 | A12 | A11 | | | |
| YOFF (P09H) | | | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |
| FR (P0AH) | | | | | F3 | F2 | F1 | F0 |
| SPUR (P0BH) | | PRE2 | PRE1 | PRE0 | | POST2 | POST1 | POST0 |
| ARTDIR (P14H) | 7/8 bits Transmit Data | | | | | | | |
| PDR (P17H) | Print Data | | | | | | | |

2.3.2 Writing to an I/O Port

The PINE OS stores the current output state of the I/O registers in the system RAM areas. The purpose of this is to allow the user to update portions of the I/O registers and to restore the I/O register data after power shut-off. When writing these registers directly from a user program, therefore, it is necessary to rewrite the contents of the corresponding system RAM areas simultaneously. The table below lists the I/O registers and the corresponding system RAM areas.

| I/O Address | Name | RAM Address | Variable Name | Remarks |
|---|---|---|---|---|
| P00H | CTLR1 | F001H | RZCTLR1 | |
| P04H | IER | F53EH | RZIER | Must be set to DI state during update. |
| P05H | BANKR | F53DH | RZBANKR | Another procedure is required when actually switching banks. |
| P15H | ARTMR | F003H | RZARTMR | |
| P16H | ARTCR | F004H | RZARTCR | |
| P18H | SWR | F005H | RZSWR | |
| P19H | IOCTLR | F006H | RZIOCTLR | |

## CHAPTER 3 7508 CPU

# CHAPTER 3 7508 CPU

This chapter describes the 7508 slave CPU commands and functions and how to transfer data to and from the 7508.

See Sections 3.5, "Keyboard" and 4.7, "Interrupts" in Part II, "Software" for details.

## 3.1 7508 CPU Functions

The 7508 CPU performs the following functions:
(1) Controlling keyboard functions such as keyboard scan.
(2) Turning on and off the main CPU switch.
(3) Controlling the RESET button.
(4) Monitoring the battery voltage and switching batteries.
(5) Performing the alarm function.
(6) Performing the 1-second interval timer function.
(7) Controlling the power switch.
(8) Controlling the calendar and clock.
(9) Controlling DRAM refreshing.
(10) Transferring serial data to and from the main CPU.

In addition to generating interrupts, the 7508 CPU transfers commands and data to and from the Z-80 CPU via a serial data line using a handshaking technique.

The processing results for functions (1) through (7) above are returned to the Z-80 in the form of interrupts. The Z-80 identifies the interrupt source by reading the 7508 status code.

## 3.2 Interfaces

### 3.2.1 I/O Ports

The PINE Z-80 CPU uses the following I/O ports when transferring data or commands to and from the 7508 CPU:

(1) Serial data communication

P06H Read (SIOR)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Data from the 7508 |

8 bits data

P06H Write (SIOR)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Commands or data to be sent to the 7508 |

8 bits data

PØ5H Read (STR)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | RDYSIO | X | X | X |

RDYSIO = Ø : Access inhibited
= 1 : Access allowed

PØ1H Write (CMDR)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | RESET RDYSIO | X |

Used to control the RDYSIO control signal.

Reset RDYSIO = Ø : Does nothing.
= 1 : Resets.

(2) Interrupt handling

PØ4H Read (ISR)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | INTO |

Used to inform the Z-8Ø CPU that an interrupt occurred in the 75Ø8.

INTØ = Ø : No interrupt has occurred.
= 1 : An interrupt has occurred.

PØ4H Write (IER)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | IERO |

Used to disable the 75Ø8 for interrupts.

IERØ = Ø : Disabled
1 : Enabled

Bits marked with X are not affected by the 75Ø8 CPU.

3.2.2 Transferring Data and Commands to and from the 7508 CPU

This subsection describes the procedures for transferring commands or data to and from the 7508 CPU.

(1) Sending commands or data to the 7508

The flowchart in Figure 3.2.1 illustrates the procedure for sending commands or data to the 7508.

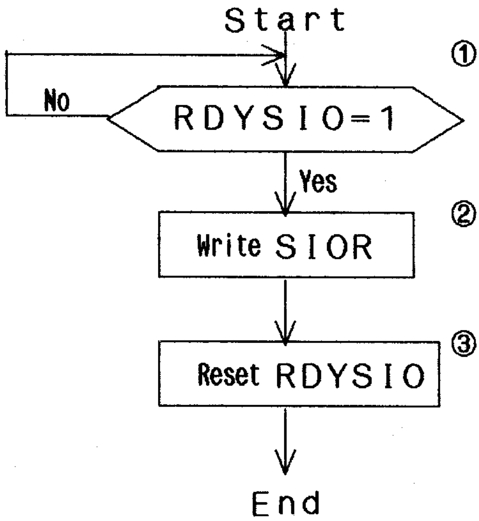



Figure 3.2.1 Procedure for Sending a Command or Data

When one or more data bytes are to be sent following the command, the above procedure is repeated the number of times equal to the number of the commands and data bytes.

| Step | Processing | Description |
|---|---|---|
| 1 | RDYSIO = 1 ? | * Read PØ5H and check whether or not the 7508 is ready to receive a command or data byte.<br>* If bit 3 = 1, go to step 2. If bit 3 = Ø, repeat step 1. |
| 2 | Write SIOR | * Write a command or data byte into PØ6H to send it to the 75Ø8. |
| 3 | Reset RDYSIO | * Reset the 75Ø8 RDYSIO signal and write Ø2H into PØ1H. |

(2) Receiving data from the 75Ø8

The flowchart in Figure 3.2.2 illustrates the procedure for receiving data from the 75Ø8 CPU.

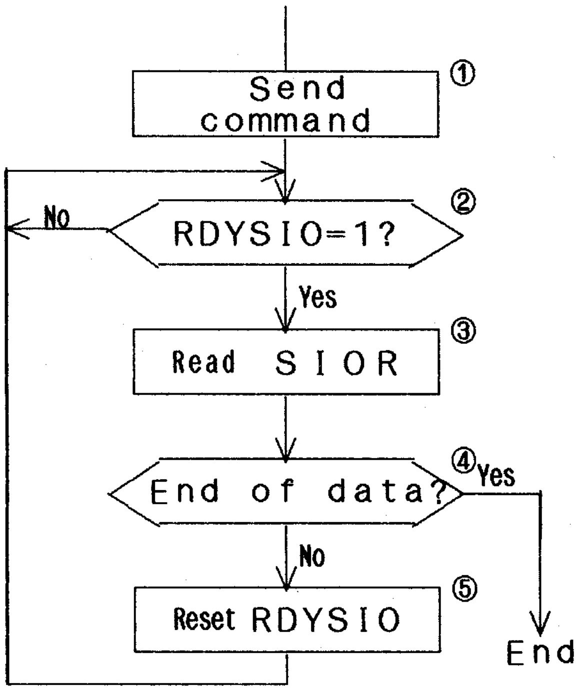



Figure 3.2.2 Procedure for Receiving Data

| Step | Processing | Description |
|---|---|---|
| 1 | Send command | * Send a command according to the flowchart in Figure 3.2.1. |
| 2 | RDYSIO = 1 ? | * Read PØ5H and check whether or not the main CPU is ready to receive data from the 75Ø8 CPU. If bit 3 = 1, go to step 3. If bit 3 = Ø, repeat step 2. |
| 3 | Read SIOR | * Read PØ6H to get data from the 75Ø8. |
| 4 | End of data? | * Check whether or not the main CPU received the number of data bytes specified in the command. Go to step 5 if there is any more data to be received. |
| 5 | Reset RDYSIO | * Reset the 75Ø8 RDYSIO signal and write Ø2H into PØ1H. |