IMS INTERNATIONAL

MODEL 440 I/O BOARD

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FUNCTIONAL DESCRIPTION

The Model 440 I/O Board serves as an integral part of the IMS 5000 and 8000 computer systems by providing timing, and I/O interfacing for two serial and one 24-BIT parallel port.

Timing is provided by the Programmable Interval Timer (PIT). The PIT is a Timer/Counter and functions as a general-purpose, multi-mode timing element that generates relative time interrupts under software control.

The Universal Asynchronous Receiver/Transmitter (UART) interfaces the Z-80 Microprocessor to an Asynchronous Serial Data Channel. The UART converts input serial data to parallel data to be acted upon by the system. Output data is converted from parallel to serial to be placed on the RS-232 PORT.

The Programmable Peripheral Interface Circuit interfaces the Z-80 Microprocessor to three 8-bit parallel ports. These parallel ports are located at the 50 pin I/O connector at the top of the 440 I/O board. Each line is TTL buffered and has provision for termination. This parallel port is programmable and can be set to input, output, or bidirectional I/O under software control.

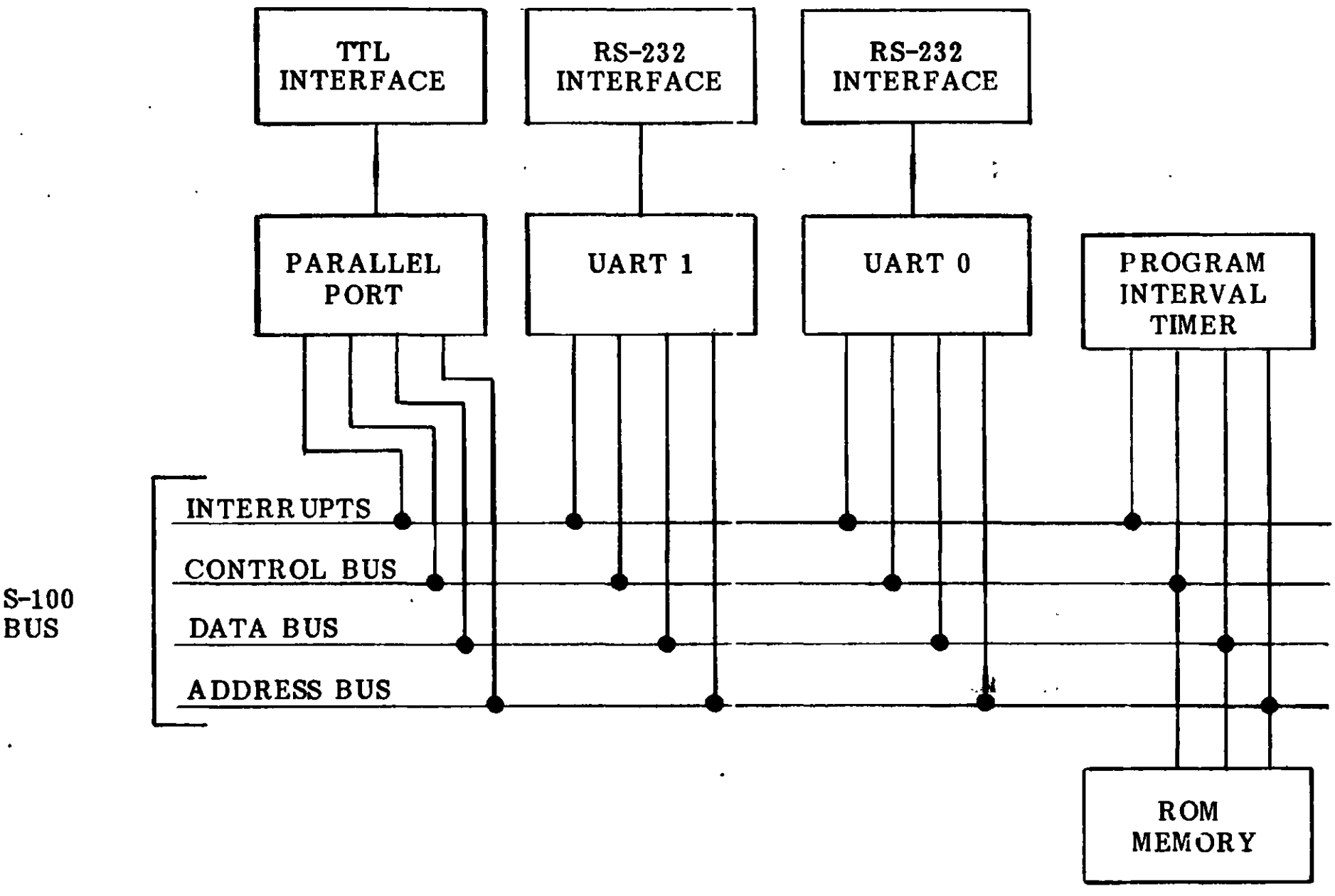
FEATURES

- 2048 by 8-bit ultraviolet Erasable Programmable Read-Only-Memory
- Programmable Interval Timer/Relative Time Clock
- Two Universal Asynchronous Receiver/Transmitters (UART's)
  Baud rates from 75 to 19.2K
- RS-232 with partial modem control
- Three 8-bit parallel ports

SPECIFICATIONS

• On-Board ROM:	Up to 4 Kbyte
• I/O Ports (Serial):	2
• 8 Bit Parallel Ports:	3
• Baud Rate:	75 to 19.2K Baud
• PCB Dimensions:	5.25" x 10" (13.3 cm x 25.4 cm)
• Power Requirements:	**Model 440** +16 @ 60 ma +8 @ 500 ma -16 @ 40 ma

FIGURE 1 - BOARD BLOCK DIAGRAM



2048 x 8 EPROM (Memory)

The 2716 is a high-speed, bit-erasable, and electrically reprogrammable Read Only Memory (EPROM), packaged in a 24-pin, Dual In-Line Package. EPROM address space is SHUNT selectable. The EPROM contains the IMS Initial Program Loader (IPL).

PROGRAMMABLE INTERVAL TIMER

The 8253 Programmable Interval Timer is a programmable Counter/Timer. The 8253 functions as a general-purpose, multi-mode timing element that can be treated as an array of I/O ports in the system software.

The 8253 allows the programmer to set up timing loops in the system software so as to generate accurate time delays under software control. The user may initialize one of the three counters with the desired quantity and, upon command, count out the delay and interrupt the CPU when it has completed its tasks. This minimizes software overhead and allows multiple delays that can be easily maintained by assignment of priority levels.

Other Counter/Timer functions provided by the 8253 are:

- Relative Time Clock
- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Digital One-Shot

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The 440 has two on-board Serial I/O Ports. Each port consists of a UART and one-third of the programmable interval timer (PIT). The UART is a programmable MOS/LSI device used for interfacing an Asynchronous Serial Communication Line to the parallel data lines of the microprocessor.

The UART is made up of two separate and independent sections:

1. The receiver
2. The transmitter

RECEIVER

The receiver accepts the serial data, converts it to parallel and decodes it. The decode function converts the serial Start, Data, Parity, and Stop bits to parallel information and verifies the proper code transmission by checking parity and the receipt of a valid stop bit.

TRANSMITTER

The transmitter section converts the parallel data into a serial word which contains the data, along with the start, parity, and stop bits.

Both the receiver and transmitter double-buffer data transfers with the processor. The UART may be programmed as follows:

1. The word length may be either 5, 6, 7, or 8 bits. (8 bits IMS standard.)
2. Parity generation and checking may be inhibited, and the parity may be odd or even. (No parity standard.)
3. The number of stop bits may be one or two (1 1/2 when transmitting a 5-bit code). (1 stop bit standard.)
4. The baud rate may be set from 75 to 19.2K baud. (9600 baud standard.)

RS-232 VOLTAGE INTERFACE

The two serial ports of the Model 440 I/O board communicate with peripherals using EIA RS-232 Voltage Interfaces. The RS-232 interface standard is for the interconnection of data processing terminal equipment and data communication equipment. It defines a means of exchanging control signals and binary serialized data signals between data processsing terminal equipment and data communications equipment, and is of particular importance when each is furnished by a different company.

Below is a summary of the IMS application which uses pins two through eight, and pin twenty. The 440 I/O board and cable are designed to look like data communication equipment so as to allow straight through wiring to a terminal (e.g. CRT or serial printer) and are wired as follows:

pin	2	=	Transmit Data	(output serial data)
pin	3	=	Receive Data	(input serial data)
pin	4	=	Request to Send	(output level set by computer)
pin	5	=	Clear to Send	(input status available to computer)
pin	7	=	Signal Ground	

The following pins are tied together at the DB-25 connectors on the internal 440 I/O cable in IMS 5000 and IMS 8000 systems:

pin	6	=	Data Set Ready	(input from remote device fed to DTR)
pin	8	=	Data Carrier Detect	(input from remote device fed to DTR)
pin	20	=	Data Terminal Ready	(output level needed by device to tell unit is reacy)

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The serial ports on board the Model 440 can be directly connected to any terminal. If you connect either of these I/O ports to a **modem**, the transmit and receive lines (pins 2 and 3) must be reversed at either end of the interconnecting RS-232 cable .

Serial port 1 (CH. 1) is normally connected to the video terminal.

Serial port 2 (CH. 2) is normally connected to the serial printer.

The 12 pin connector (top center of the 440 I/O board) connects the two UART's on the Model 440 I/O board to the two DB25 female connectors mounted on the I/O panel at the rear of the IMS computer (CH. 1 and CH. 2). The internal cable connecting this 12 pin connector and the two female DB25 connectors is wired as follows:

12 Pin Connector	**Definition**	**DB25 (CH. 1 - Console Port)**
Pin #	Is Connected To	Pin #
1 (TX)	Transmit Data	**3**
2 (RD)	Receive Data	**2**
3 (CTS)	Clear to Send	**5**
4 (RTS)	Request to Send	**4**
5 (GND)	Signal Ground	**7**
		DB25 (CH. 2 - Printer Port)
6 (GND)	Signal Ground	**7**
7 (RTS)	Request to Send	**4**
8 (CTS)	Clear to Send	**5**
9 (RD)	Receive Data	**2**
10 (TX)	Transmit Data	**3**

For the following discussion, "**X**" refers to the base address at which the Model 440 I/O board is configured. For example, if pins "A7, A6, and A5" are shunted at pad "**JP**" and pin "A4" is not shunted, the board would be configured for an address of 10 hex. "**X**" in this case would be "1". If the board is addressed at 20 hex, "A7,A6,A4" shunted and "A5" unshunted, then "**X**" would be "2". If pins "A7, A5, A4" are shunted and "A6" unshunted, then "**X**" would be "4" and the base address of the board would be 40 hex. **Note:** The Model 440 I/O board is normally shunted at the factory for an address of 10 hex.

PORT CONTROL - Port X8H interrupt mask, request-to-send, and ROM enable bit assignments are as follows:

BIT	DESCRIPTION
0	ROM disabled = 1
1	Relative Time Clock interrupt enable =1
2	UART 1 transmit interrupt enable = 1
3	UART 1 receive interrupt enable = 1
4	UART 1 request-to-send
5	UART 0 transmit interrupt enable = 1
6	UART 0 receive interrupt enable = 1
7	UART 0 request-to-send

The Relative Time Clock (RTC) interrupt (bit 1) is reset when out X9H is executed.

The EPROM Enable/Disable (bit 0) shunt is located at Pad JG "RE".

UART CONTROL - Control for UART 0 is accomplished by the following line and bit assignments:

BIT	FUNCTION
Out X0H= Control	
0	Parity Inhibit
1	Even Parity Enable
2	Stop Bit Select
3	Word Length - LSB
4	Word Length - MSB
Out X1H= Transmitted Data	
In X0H= Status	
0	Receive Data Available (RDA)
1	Transmit Buffer Empty (TBE)
2	Parity Error
3	Framing Error
4	Overrun Error
7	Clear-To-Send
In X1H= Received Data	

Line and bit assignments for UART 1 are as follows:

Out X2H= Control
Out X3H= Transmitted Data
 In X2H= Status
 In X3H= Receive Data
(Bit assignments are the same as UART 0)

PIT CONTROL - The Programmable Interval Timer provides three independent counters for interrupt timing:

Counter 0	UART 0 Baud Clock
Counter 1	UART 1 Baud Clock
Counter 2	Relative Time Clock

Output X7H provides control for the PIT. An out to X7H must be accomplished before establishing the timing intervals for each counter. The division factor is loaded into each count register to establish the desired frequency output. The base clock frequency is 2MHz if pins 1 and 4 are shunted at pad JH (for baud rates of 75 to 9600). The base clock frequency is 1.2288 MHz if pins 2 and 3 are shunted instead (for baud rates of 75 to 19200). The following values should be output to port X7H for each counter as follows:

COUNTER	OUTPUT
0	36H
1	76H
2	B6H

The following routine can be used to initialize the real time clock:

```
MVI   A,0B6H    ; write control word for counter 2
OUT   17H
MVI   A,28H     ; set counter 2 LSB
OUT   16H
MVI   A,82H     ; set counter 2 MSB
OUT   16H
OUT   19H       ; reset RTC interrupt and start counting
MVI   A,3H      ; unmask interrupt and disable EPROM
OUT   18H
```

To load the count registers, the desired division rate should be output (least significant byte first) for the counter as follows:

COUNTER	OUTPUT
0	Port X4H
1	Port X5H
2	Port X6H

The algorithm for determining the Baud Rate for the UARTs is as follows, using Baud 9600 for the example:

$$\frac{\text{Input Frequency}}{\text{Baud x 16}} = \frac{1{,}228{,}800}{9600 \times 16} = 0008H$$

Note that the UART requires an input frequency of 16 times the Baud Rate.

So: Output 36H to port X7, then
Output 08H to port X4, then
Output 00H to port X4

The following routine is used to initialize UART 0:

```
MVI     A,36H     ; select UART 0 counter
OUT     17H
MVI     A,08H     ; set baud to 9600 LSB
OUT     14H
MVI     A,0H      ; set baud to 9600 MSB
OUT     14H
MVI     A,19H     ; set inhibit parity  1 stop bit  8 bit character
OUT     10H
```

UART 0 is now set to run at 9600 baud with the 1.2288 MHz OSC enabled.

PROGRAMMABLE PERIPHERAL INTERFACE

The Intel 8255A is a general purpose programmable I/O device. It is used in the IMS system to interface parallel peripheral equipment to the microcomputer S-100 bus. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode, MODE 0, each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In the second mode, MODE 1, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation, MODE 2, is a bi-directional bus mode which uses 8 lines for a bi-directional bus, and 5 lines, borrowing one from the other group, for handshaking.

The functional configuration of each port is programmed by the system software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

There are three basic modes of operation that can be selected by the system software:

MODE 0 - Basic Input/Output

MODE 1 - Strobed Input/output

MODE 2 - Bi-Directional Bus

MODE 0 This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required. Data is simply written to or read from a specified port.

MODE 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different I/O configurations are possible in this mode

MODE 1 This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accecpt these "handshaking" signals.

MODE 1 Basic Functional Definitions:

- Two groups (group A and group B)
- Each group contains one 8-bit data port and one 4-bit control/data port
- The 8-bit data port can be either input or output
  Both inputs and outputs are latched
- The 4-bit port is used for control and status of the 8-bit data port

MODE 2 This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (Bi-Directional). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

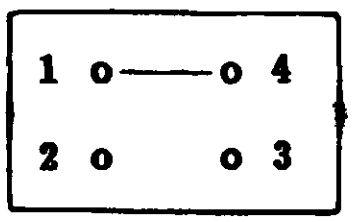
MODE 2 Basic Functional Definitions:

- Used in group A only
- One 8-bit, bi-directional port (A) and a 5-bit control port (C)
- Both inputs and outputs are latched
- The 5-bit control port (C) is used for control and status for the 8-bit bi-directional port (A)

If you need more detailed programming information regarding the 8255A, we suggest you consult the Intel Peripheral Design Handbook.

CONFIGURING THE 440 I/O BOARD

PARALLEL PORT A SELECT (PAD JA)



No shunts = input mode

Shunt JA 1-4 = output

Shunt JA 2-3 = bi-directional mode

PARALLEL PORT A DRIVER/RECEIVER (BOARD LOCATION 8A, 10A)

74LS243 non inverting

74LS242 inverting

PARALLEL PORT A TERMINATION OPTIONS (BOARD LOCATION 9A)

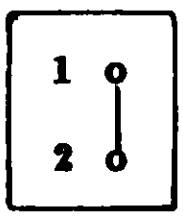
Open = No termination

Use a Beckman* 899-1-R1.0K For Pull Up

Use a Beckman 899-5-R220/330 For Pull Up/Down

2 = Resistor Network

PARALLEL PORT B SELECT (PAD JB)



No shunt = input mode

Shunt JB 1-2 = output mode

PARALLEL PORT B DRIVER/RECEIVER (BOARD LOCATION 10B, 11A)

74LS243 non inverting

74LS242 inverting

PARALLEL PORT B TERMINATION OPTIONS (BOARD LOCATION 11B)

Open = No termination

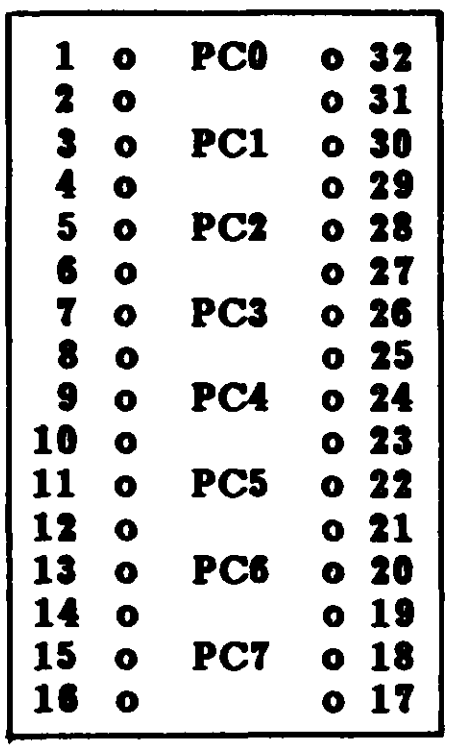
Use a Beckman 899-1-R1.0K For Pull Up

Use a Beckman 899-5-R220/330 For Pull Up/Down

* BECKMAN = Hersteller von Widerstandsnetzwerken

CONFIGURING THE 440 I/O BOARD

PARALLEL PORT C SELECT (PAD JC)



Port C is bit selectable.
Each bit is selected individually depending on the programming of the 8255.

No shunts = Bit unused

Horizontal shunts = output (driver)

Vertical shunts = input (receiver)

PARALLEL PORT C DRIVER/RECEIVER (BOARD LOCATION 13A)

74LS244 non inverting

74LS240 inverting

PARALLEL PORT C TERMINATION OPTIONS (BOARD LOCATION 12A)

Open = no termination

Use a Beckman 899-1-R1.0K For Pull Up

Use a Beckman 899-5-220/330 For Pull Up/Down

2 Resistor Network

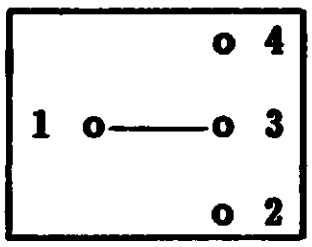
CONFIGURING THE 440 I/O BOARD

ROM SELECT (PADS JD, JE, JF, JG)

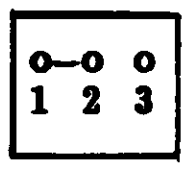
Any connections made by etch which are not defined in the following diagrams should be cut.

To Use a 2708 1K x 8 EPROM:

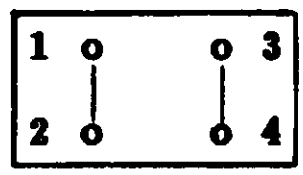
JD



JE

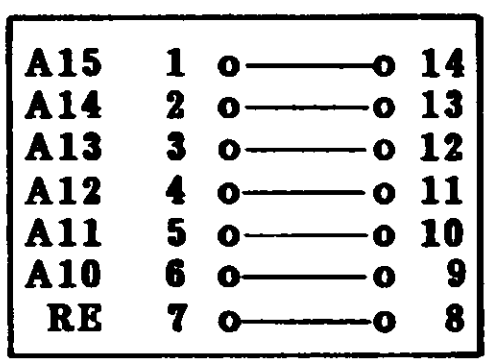


JF



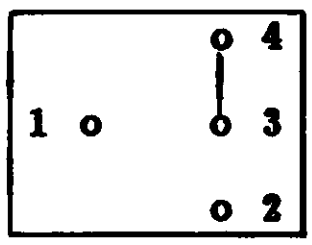
Shunt JD 1-3
Shunt JE 1-2
Shunt JF 1-2
Shunt JF 3-4
Shunt all horizontally at JG

JG

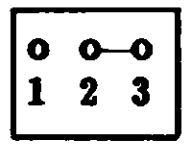


To Use a 2716 2K x 8 EPROM:

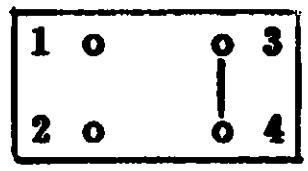
JD



JE

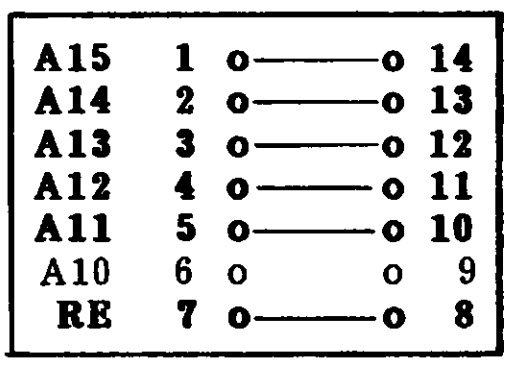


JF



Shunt JD 3-4
Shunt JE 2-3
Shunt JF 3-4
Remove shunt A10 at JG

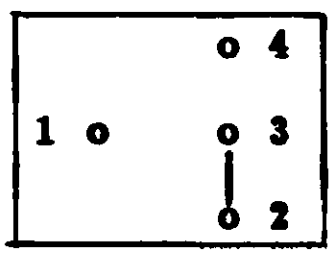
JG



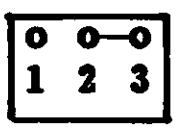
CONFIGURING THE 440 I/O BOARD

To Use a 2732 4K x 8 PROM:

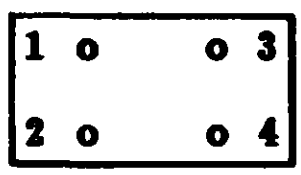
JD



JE

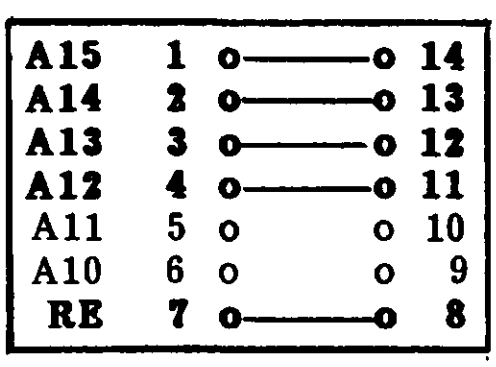


JF



Shunt JD 2-3
Shunt JE 2-3
No shunts at JF
Remove shunts A10 and A11 at JG

JG



EPROM Address Select (Pad JG)

JG

A15	**1**	**o**	**o 14**
A14	**2**	**o**	**o 13**
A13	**3**	**o**	**o 12**
A12	**4**	**o**	**o 11**
A11	**5**	**o**	**o 10**
A10	**6**	**o**	**o 9**
RE	7	o	o 8

Shunt OFF = 1 Shunt ON = 0

All Shunts OFF = EPROM Starting Address X' FC00'

All Shunts ON = EPROM Starting Address X' 0000'

EPROM Enable (RE at Pad JG)

JG

A15	1	o	o 14
A14	2	o	o 13
A13	3	o	o 12
A12	4	o	o 11
A11	5	o	o 10
A10	6	o	o 9
RE	**7**	**o**	**o 8**

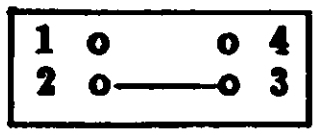
Shunt OFF "RE" = EPRCM Disabled

Shunt ON "RE" = EPROM Enabled

CONFIGURING THE 440 I/O BOARD

Timer Clock Option (Pad JH)

JH

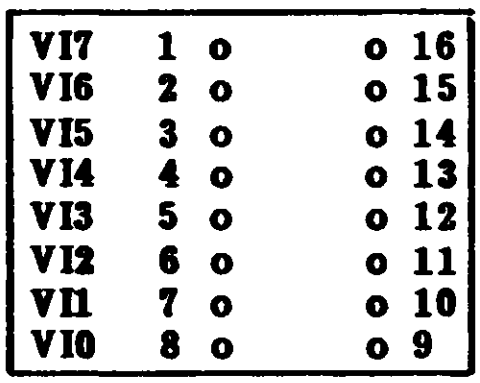


Shunt JH 1-4 = Enable External 2Mhz Clock (75 to 9600 baud rate)
Shunt JH 2-3 = Enable on-board 1.2288 Mhz Clock (75 to 19200 baud rate)

Interrupt Options (Pads JJ, JK, JL, JM, JN)

The installing of a horizontal shunt will attach the selected interrupt level to the function as defined below:

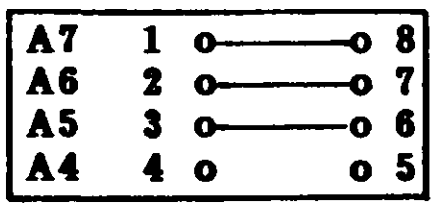
JJ - JN



JJ = Relative Time Clock (RTC) Interrupt
JK = Line 0 Transmit/Receive Interrupt
JL = Line 1 Transmit/Receive Interrupt
JM = Parallel Port B Interrupt
JN = Parallel Port A Interrupt

I/O Device Address Select (Pad JP)

JP



Shunt OFF = 1 Shunt ON = 0
All Shunts OFF = I/O Address X'F0' - X'FF'
All Shunts ON = I/O Address X'00' - X'0F'

Example:

Shunt A7, A6, A5 = I/O Address of 10 hex (Standard)
Shunt A7, A6, A4 = I/O Address of 20 hex
Shunt A7, A5, A4 = I/O Address of 40 hex

I/O DEVICE ADDRESS

X0	COMM	0	READ/WRITE CONTROL	UART 0
X1	COMM	0	READ/WRITE DATA	UART 0
X2	COMM	1	READ/WRITE CONTROL	UART 1
X3	COMM	1	READ/WRITE DATA	UART 1
X4	TIMER	0	READ/WRITE DATA (BAUD CLOCK X 16 COMM 0)	
X5	TIMER	1	READ/WRITE DATA (BAUD CLOCK X 16 COMM 1)	
X6	TIMER	2	READ/WRITE DATA (RTC)	
X7	TIMER CONTROL WRITE			
X8	INTERRUPT ENABLE/REQUEST TO SEND CONTROL			
X9	TIMER	2	INTERRUPT RESET (RTC)	
XA				
XB				
XC	PARALLEL PORT A READ/WRITE DATA			
XD	PARALLEL PORT B READ/WRITE DATA			
XE	PARALLEL PORT C READ/WRITE DATA			
XF	PARALLEL CONTROL WRITE			

X = BASE ADDRESS SELECTED AT PAD JP (If 10H then X=1, if 20H then X=2)

PIN LISTING FOR THE 440 I/O BOARD PARALLEL PORT CONNECTOR

1.	+5VDC	2.	+5VDC
3.	PA7	4.	GND
5.	PA6	6.	GND
7.	PA5	8.	GND
9.	PA4	10.	GND
11.	PA3	12.	GND
13.	PA2	14.	GND
15.	PA1	16.	GND
17.	PA0	18.	GND
19.	PB7	20.	GND
21.	PB6	22.	GND
23.	PB5	24.	GND
25.	PB4	26.	GND
27.	PB3	28.	GND
29.	PB2	30.	GND
31.	PB1	32.	GND
33.	PB0	34.	GND
35.	PC7	36.	GND
37.	PC6	38.	GND
39.	PC5	40.	GND
41.	PC4	42.	GND
43.	PC3	44.	GND
45.	PC2	46.	GND
47.	PC1	48.	GND
49.	PC0	50.	GND

PAX = PARALLEL PORT A BITS
PBX = PARALLEL PORT B BITS
PCX = PARALLEL PORT C BITS

STANDARD FACTORY ASSIGNMENTS
AS CONFIGURED FOR CP/M 2.2 AND MP/M 1.1

INTERRUPTS

		Prior to 9/1/81	After 9/1/81
VI0	00H	Reserved by CP/M	Reserved by CP/M
VI1	08H	NOT USED	Relative Time Clock
VI2	10H	Memory Parity	Memory Parity
VI3	18H	NOT USED	Communications
VI4	20H	MP/M DDT	Winchester & Hard Disk
VI5	28H	Floppy & Hard Disk	Floppy Disk
VI6	30H	Communications	Reserved for Customer Use
VI7	38H	Relative Time Clock	Reserved by CP/M for DDT/SID

I/O DEVICE ADDRESS (I/O BOARD AT BASE ADDRESS OF 10 HEX)

10H COMM 0 READ/WRITE CONTROL

11H COMM 0 READ/WRITE DATA

12H COMM 1 READ/WRITE CONTROL

13H COMM 1 READ/WRITE DATA

14H TIMER 1 READ/WRITE

15H TIMER 1 READ/WRITE

16H TIMER 2 READ/WRITE

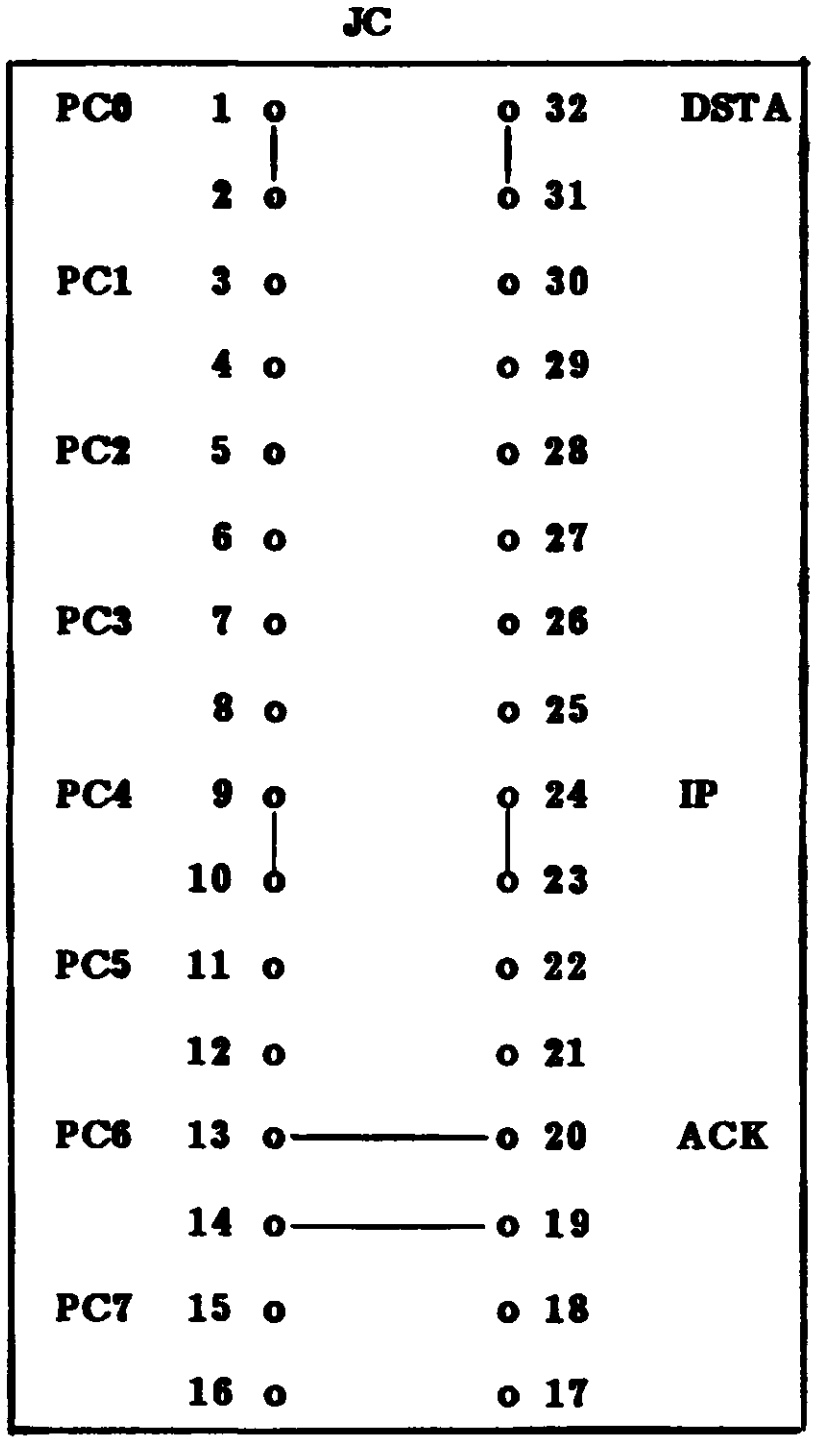
17H TIMER CONTROL

18H RTC INTERRUPT MASK AND EPROM ENABLE/DISABLE

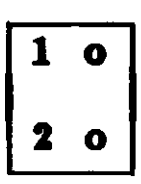
19H RTC FLIP FLOP DISABLE

PROPER SHUNTING FOR A CENTRONICS PARALLEL PRINTER

1. Shunt the following pins located at pad JC:

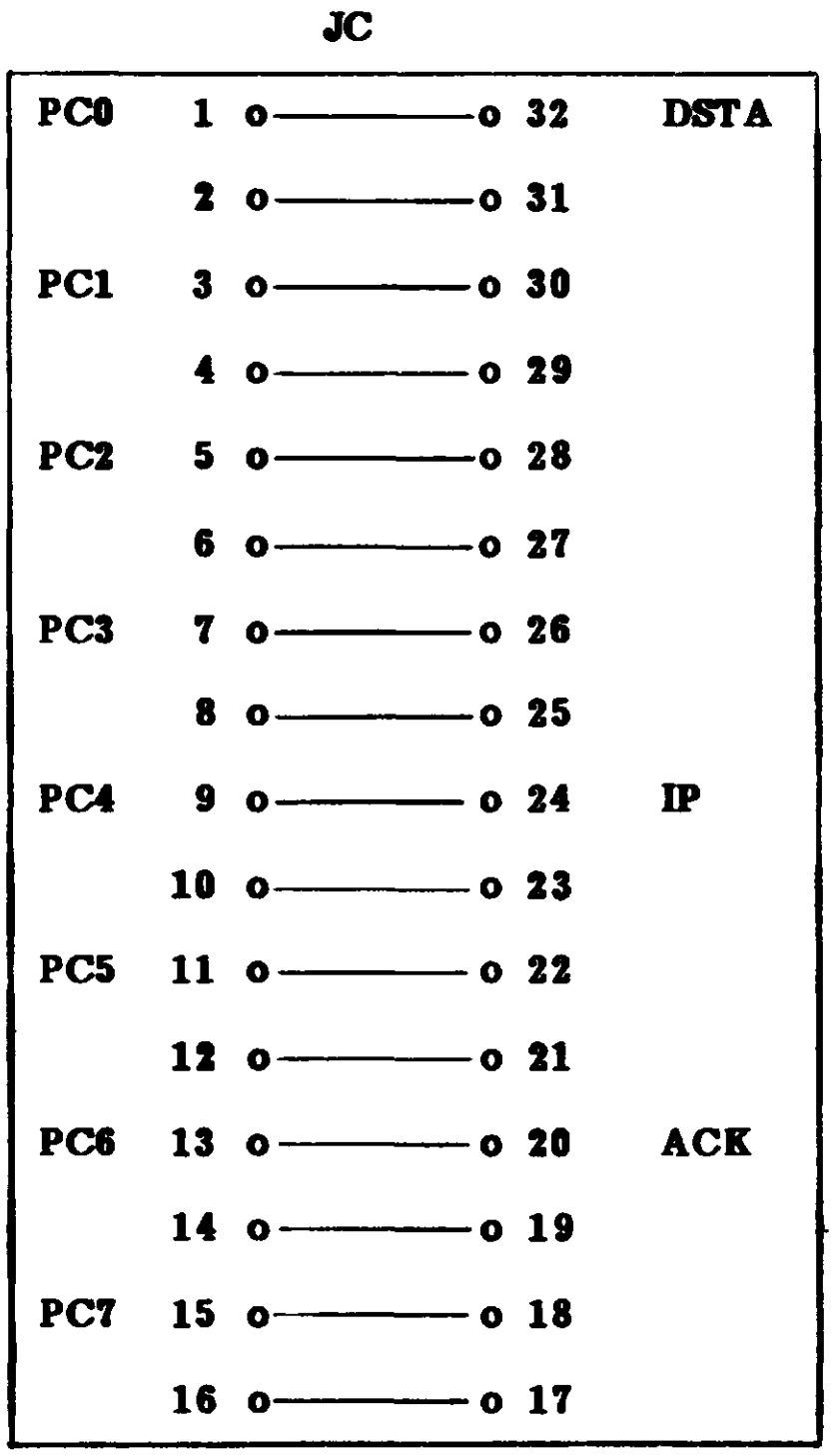


2. Remove shunt at pad JB.

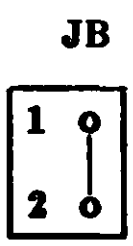


PROPER SHUNTING FOR A NEC SPINWRITER 5500D PARALLEL PRINTER

1. Install 16 horizontal shunts at pad JC (all pins shunted).



2. Install a vertical shunt at pad JB.



PARALLEL CENTRONICS PRINTER CABLE

IMS COMPUTER		CENTRONICS PRINTER	
PA7	3	9	DS8
GND	4	27	GND
PA6	5	8	DS7
GND	6	26	GND
PA5	7	7	DS6
GND	8	25	GND
PA4	9	6	DS5
GND	10	24	GND
PA3	11	5	DS4
GND	12	23	GND
PA2	13	4	DS3
GND	14	22	GND
PA1	15	3	DS2
GND	16	21	GND
PA0	17	2	DS1
GND	18	20	GND
PB3	27	11	BUSY
GND	28	29	GND
PB2	29	12	PE
PB1	31	13	SLCT
PB0	33	32	FAULT
GND	34	17	GND
PC6	37	10	ACK -
GND	38	28	GND
PC4	41	31	IP -
GND	42	30	GND
PC0	49	1	DSTA -
GND	50	19	GND

14 TWISTED PAIR CABLE

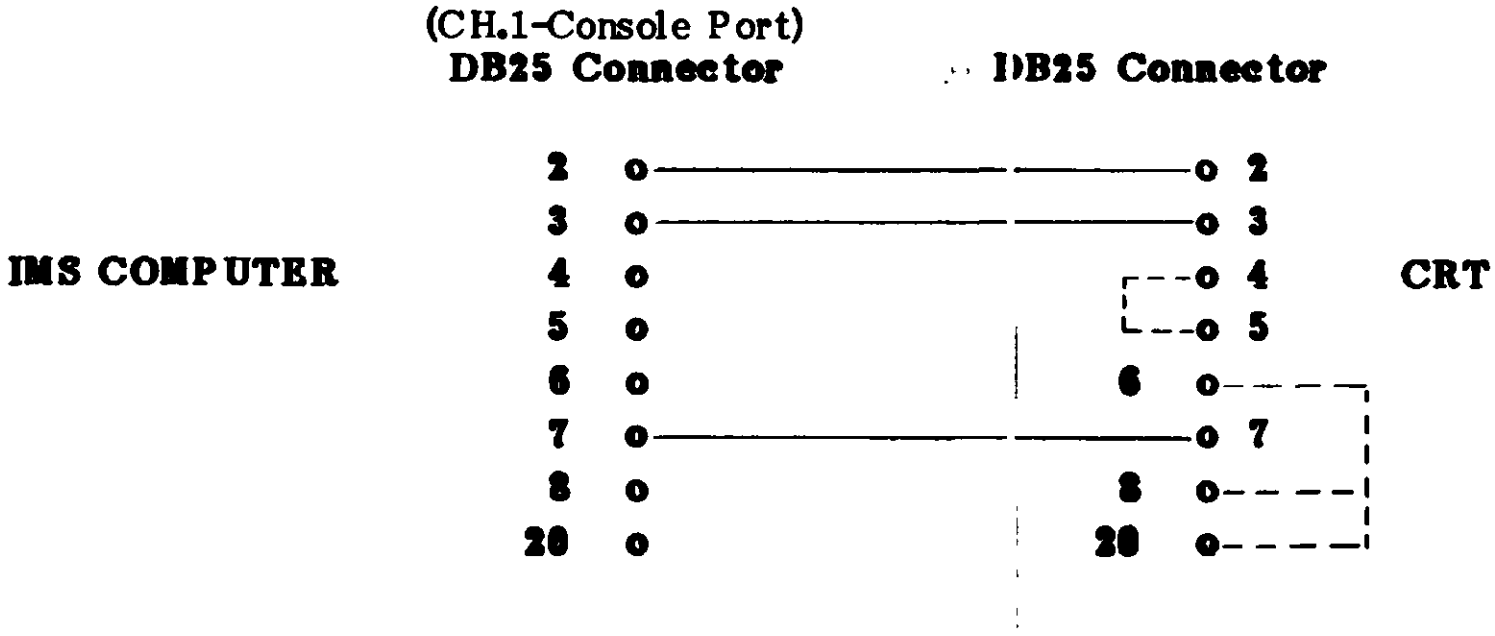
IMS CONNECTOR	CENTRONICS CONNECTOR
50 PIN IDS CONNECTOR (INSULATION DISPLACEMENT SOCKET CONNECTOR)	AMPHENAL CONNECTOR 57-30360

PARALLEL NEC SPINWRITER PRINTER CABLE

IMS Computer	NEC Spinwriter Printer	Signal
3	45	Dataline 8
5	43	Dataline 7
7	42	Dataline 6
9	40	Dataline 5
11	33	Dataline 4
13	39	Dataline 3
15	36	Dataline 2
17	37	Dataline 1
19	10	Dataline 12
21	13	Restore
23	17	Carriage Strobe
25	15	Paper Feed Strobe
27	21	Print Wheel Strobe
29	9	Dataline 11
31	1	Dataline 10
33	46	Dataline 9
35	12	Check Status
37	3	Paper Out Status
39	4	Ribbon Out Status
41		(NOT USED)
43	27	Print Wheel Ready
45	34	Paper Feed Ready
47	26	Carriage Ready
49	28	Printer Ready

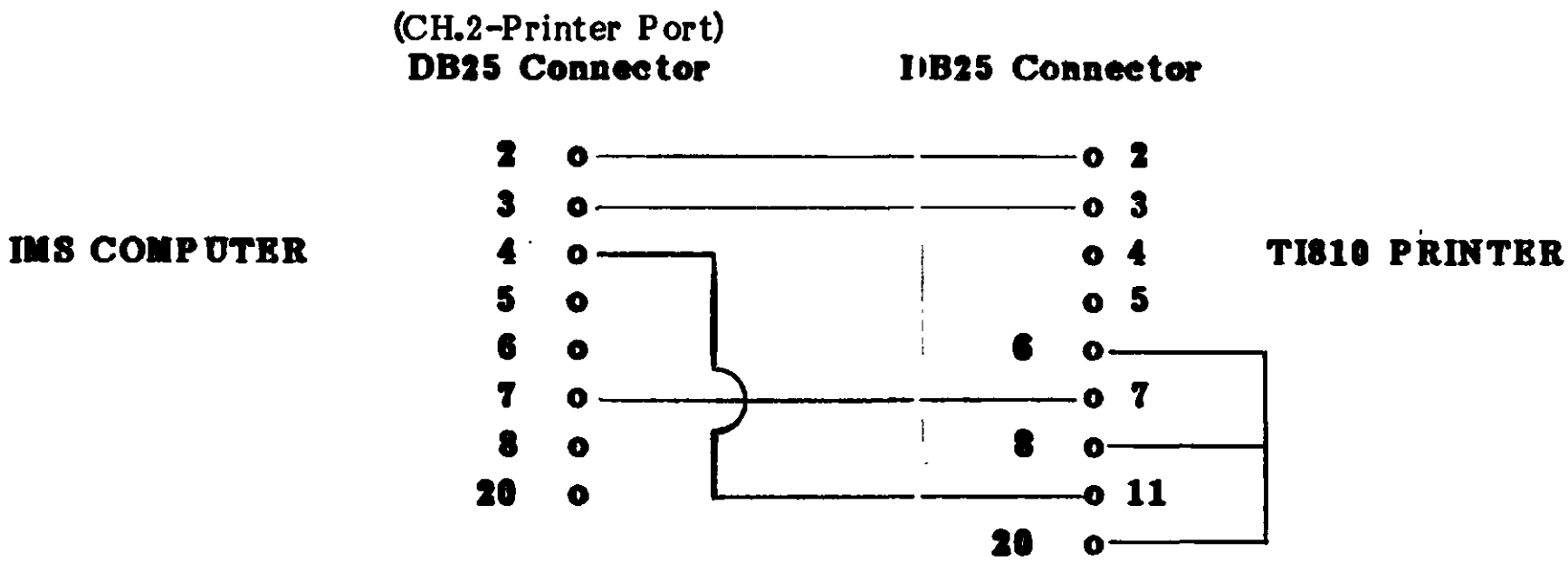
Connectors: 50 Pin IDS Connector at each end.

IMS RS232 CRT CABLE



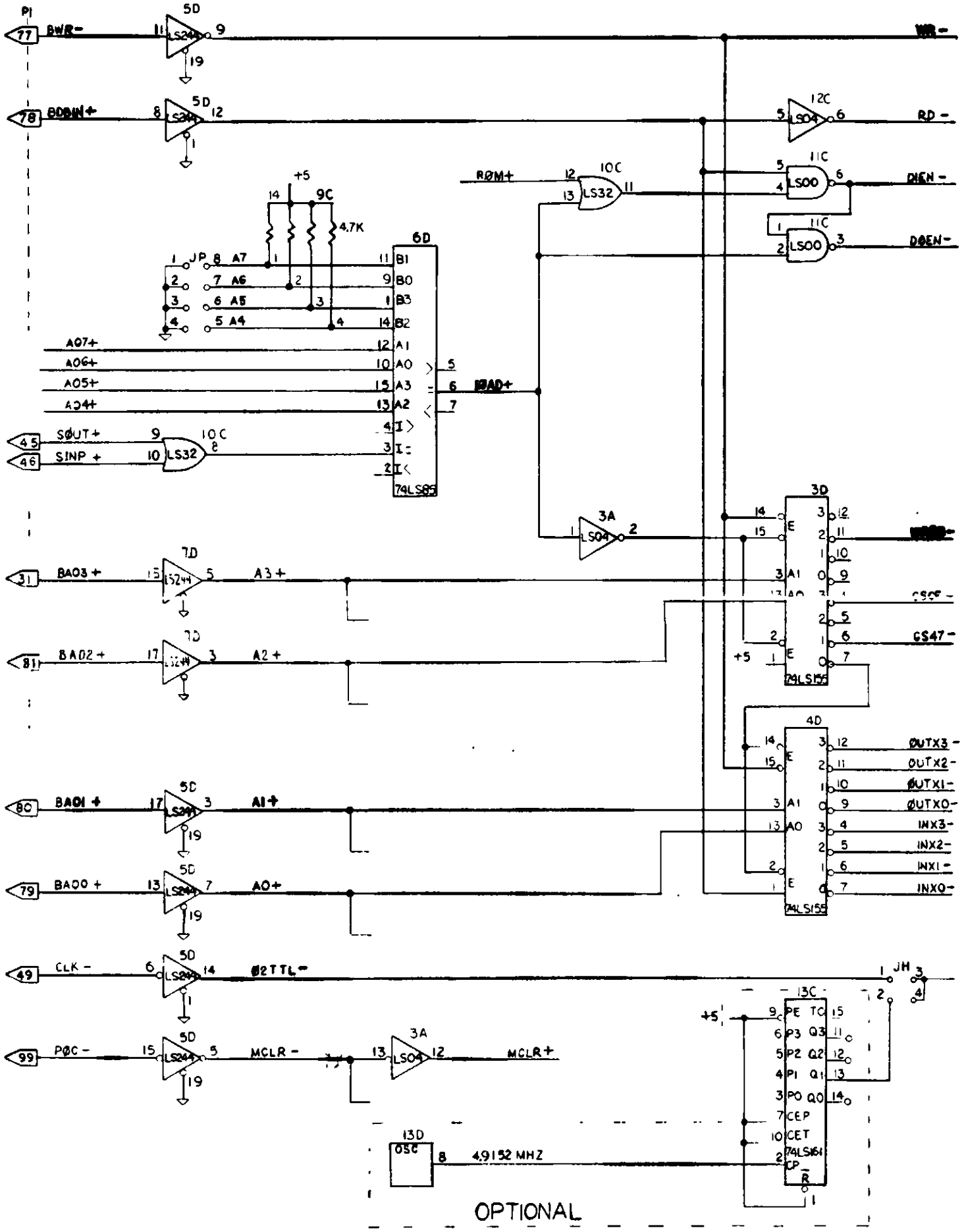
Note: Refer to the CRT manual to determine if it is necessary to tie pins 4 and 5 and pins 6, 8, and 20 together. This requirement will vary from one CRT manufacturer to another.

IMS RS232 TI810/820 PRINTER CABLE

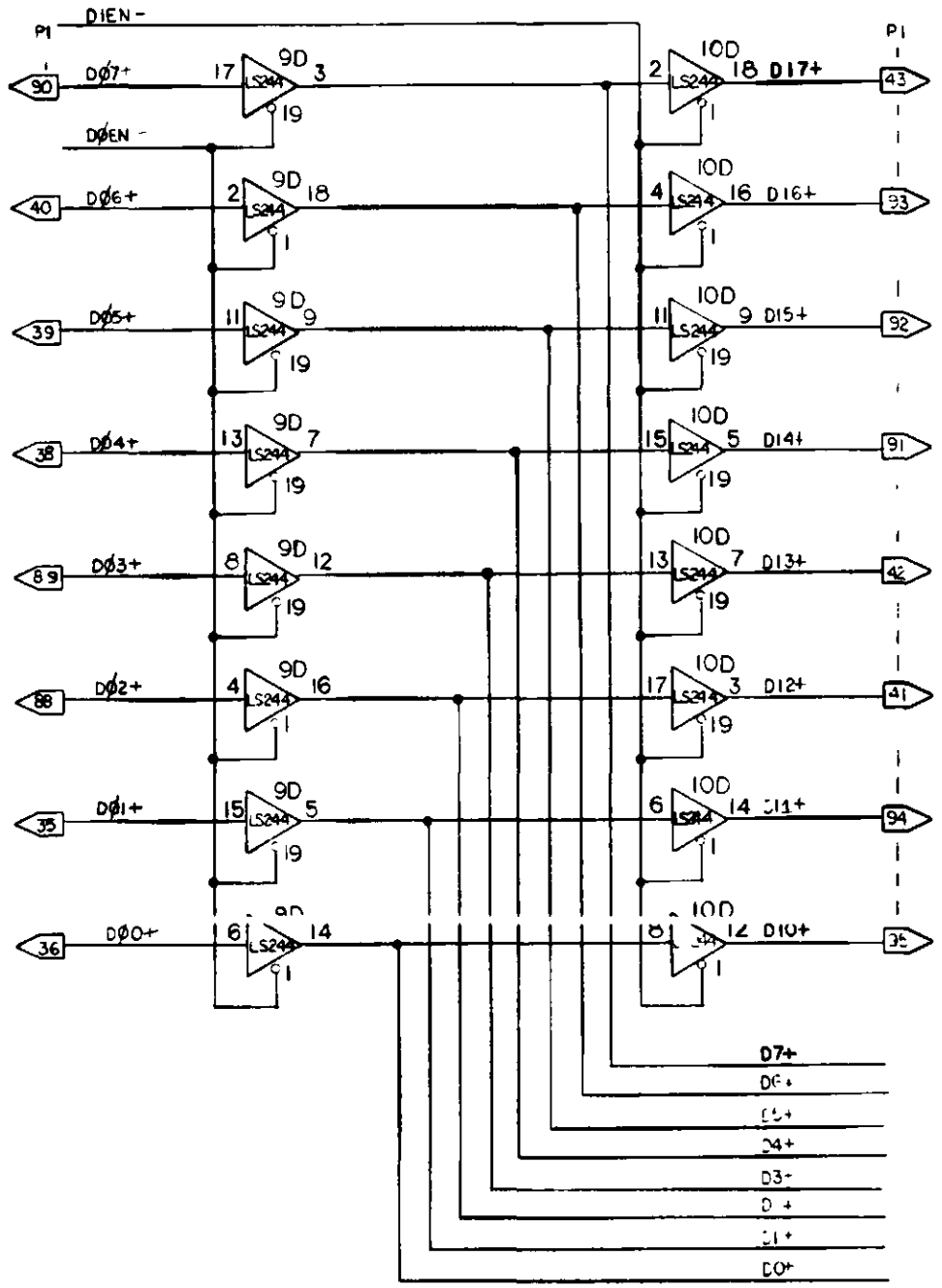


STANDARD FACTORY SHUNT CONFIGURATIONS FOR 440 I/O BOARD

Pad	Description	Standard Configuration
JA	Parallel Port A Mode Select	Shunt 1-4
JB	Parallel Port B Mode Select	Shunt 1-2
JC	Parallel Port C Select	Shunt all 16 pins horizontally
JD	EPROM Select	Shunt 3-4
JE	EPROM Select	Shunt 2-3
JF	EPROM Select	Shunt 3-4
JG	EPROM Address Select	Shunt all except 'A10' (Address 0000H)
JH	Optional Oscillator Enable	Shunt 2-3 = 75 to 19200 Baud
JJ	Relative Time Clock Interrupt	Shunt vector interrupt 1
JK	Line 0 Trans/Rec Interrupt	Shunt vector interrupt 3
JL	Line 1 Trans/Rec Interrupt	Shunt vector interrupt 3
JM	Parallel port B interrupt	No shunts
JN	Parallel port A interrupt	No shunts
JP	I/O Address Select	Shunt all except 'A4' = 10 Hex



INDUSTRIAL MICRO SYSTEMS		
SCALE NONE	APPROVED BY:	DRAWN BY
DATE 4-12-79		REVISED OCT. 9, 81
I/O BOARD		
L-A00442		DRAWING NUMBER 1 OF 9



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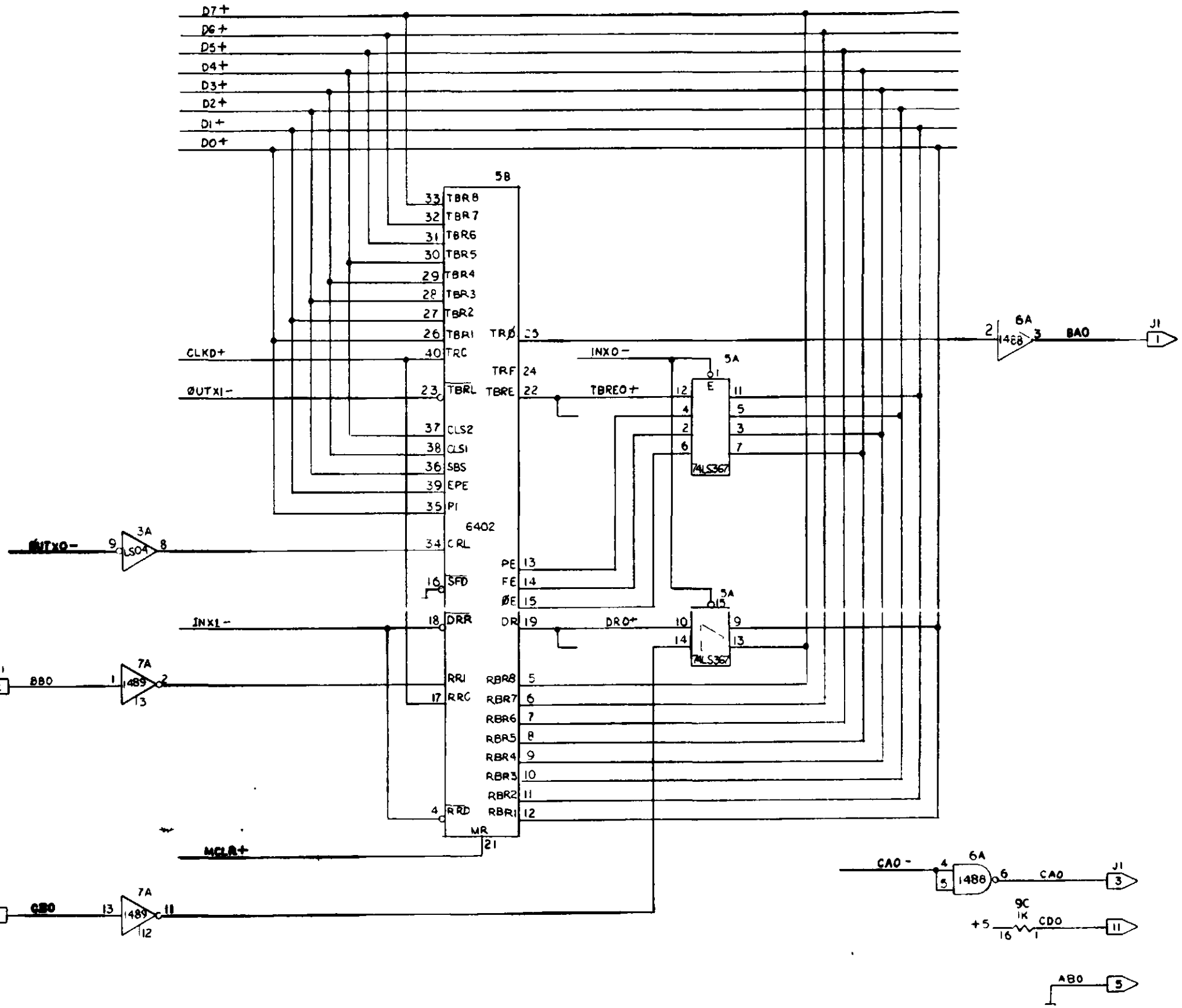
DATE 4-12-7[illegible]		REVISED
I/O BOARD		
L-A00+42		DRAWING NUMBER [illegible] OF 9



6402
VCC 1
GND 3

1488
VCC - 14 - +12
VEE - 1 - -12
GND - 7

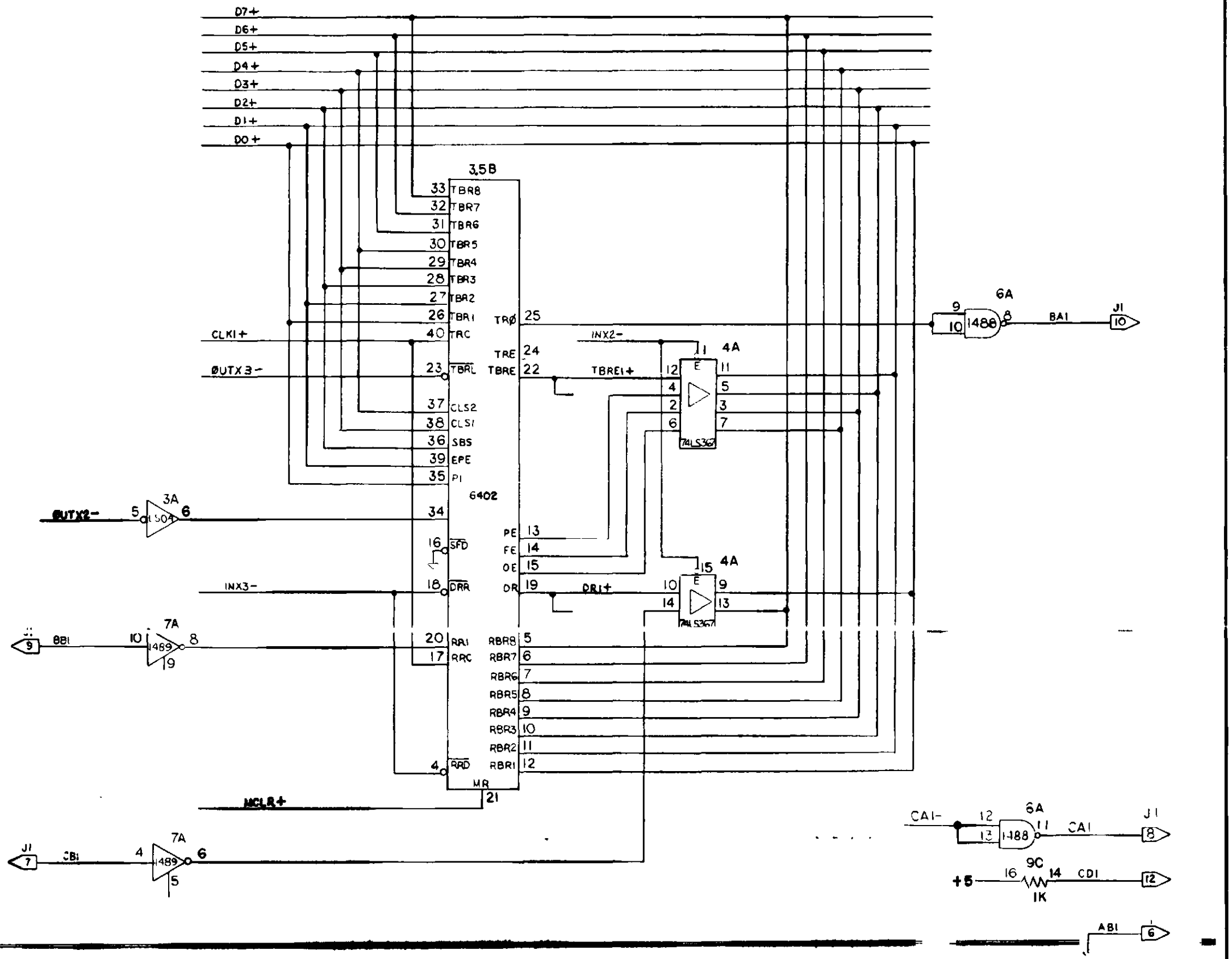
INDUSTRIAL MICRO SYSTEMS

SCALE NONE	APPROVED BY	DRAWN BY
DATE 4-12-79		REVISED July 22, 81

I/O BOARD

L-A00442

DRAWING NUMBER 2 OF 9



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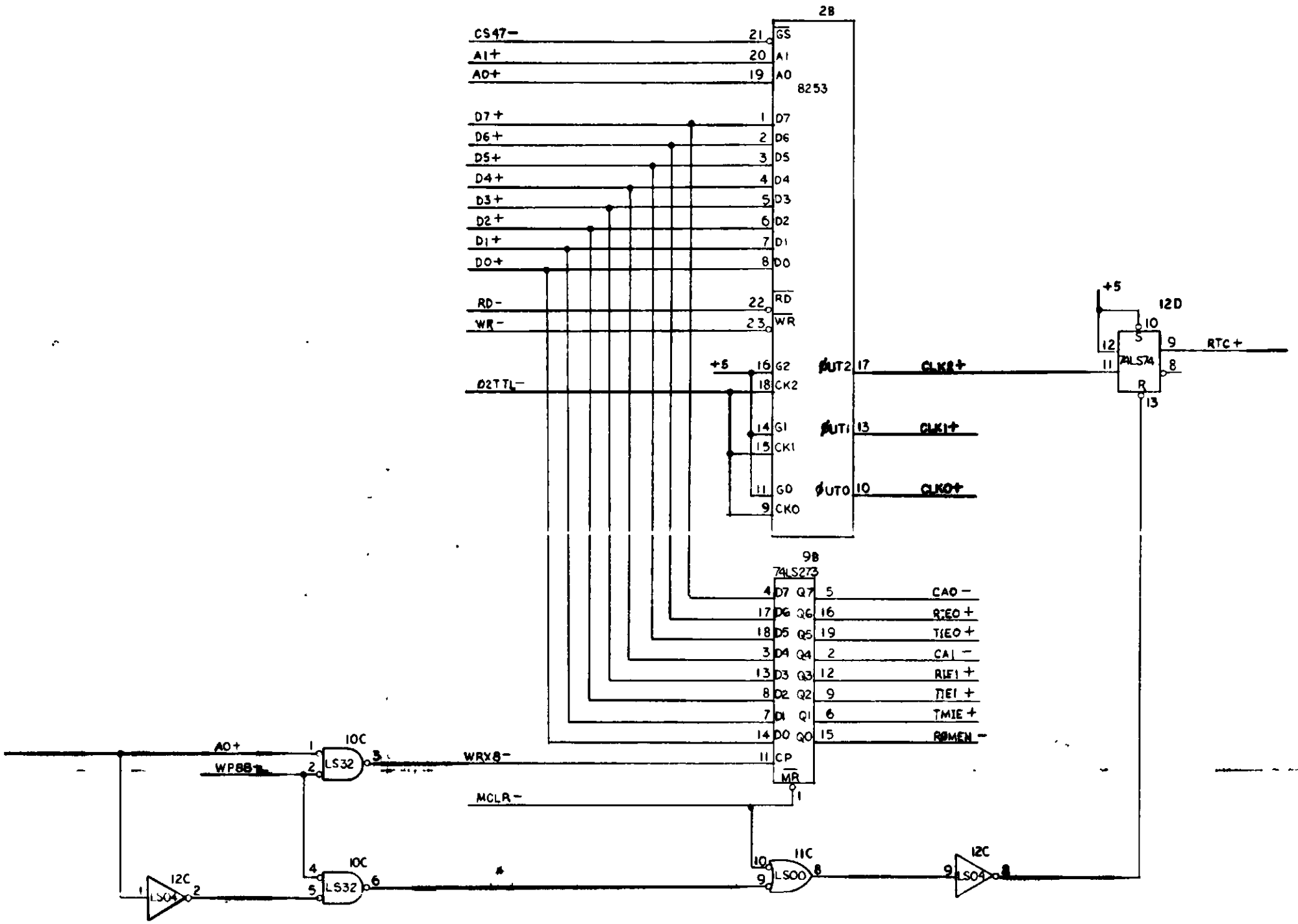
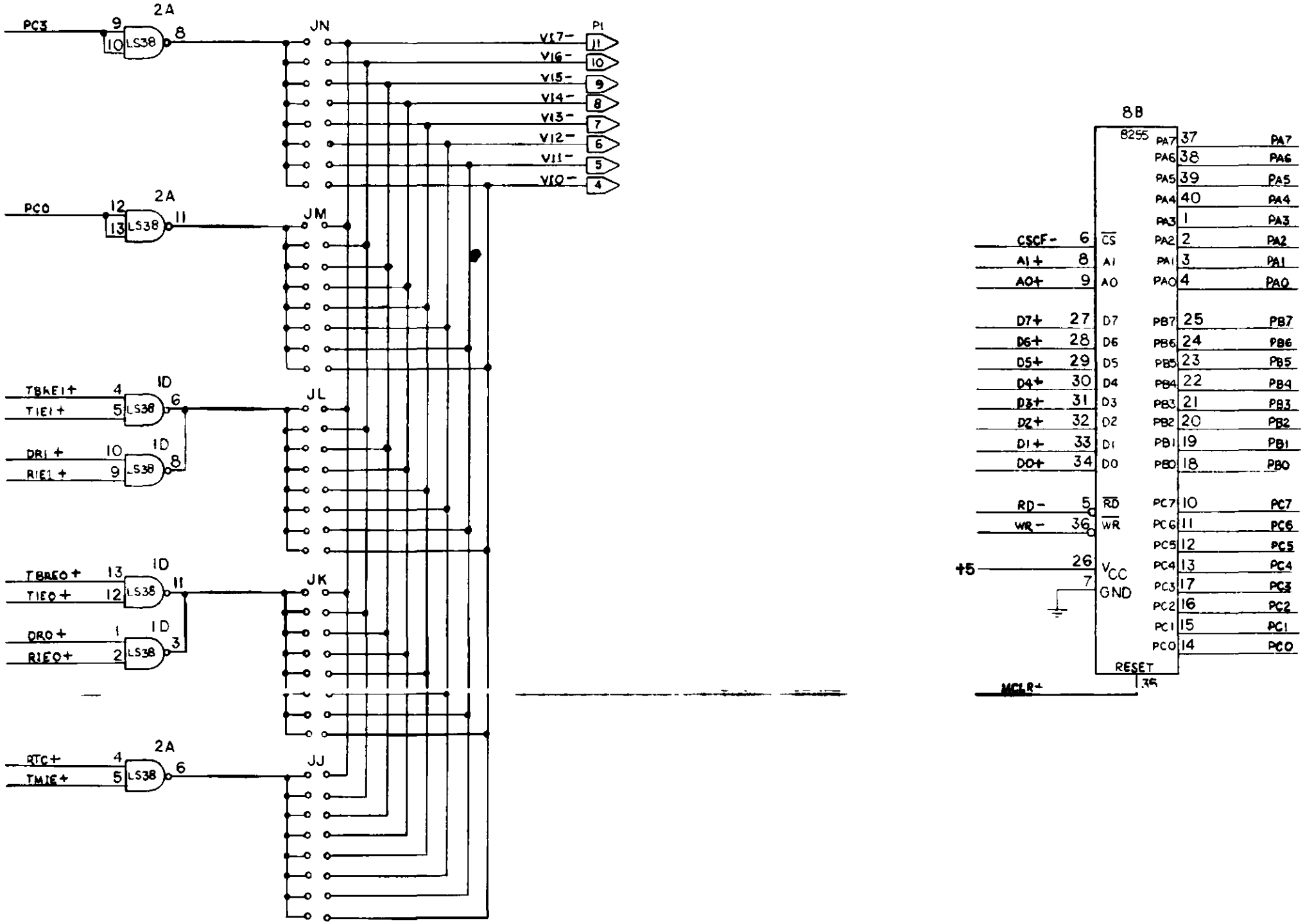
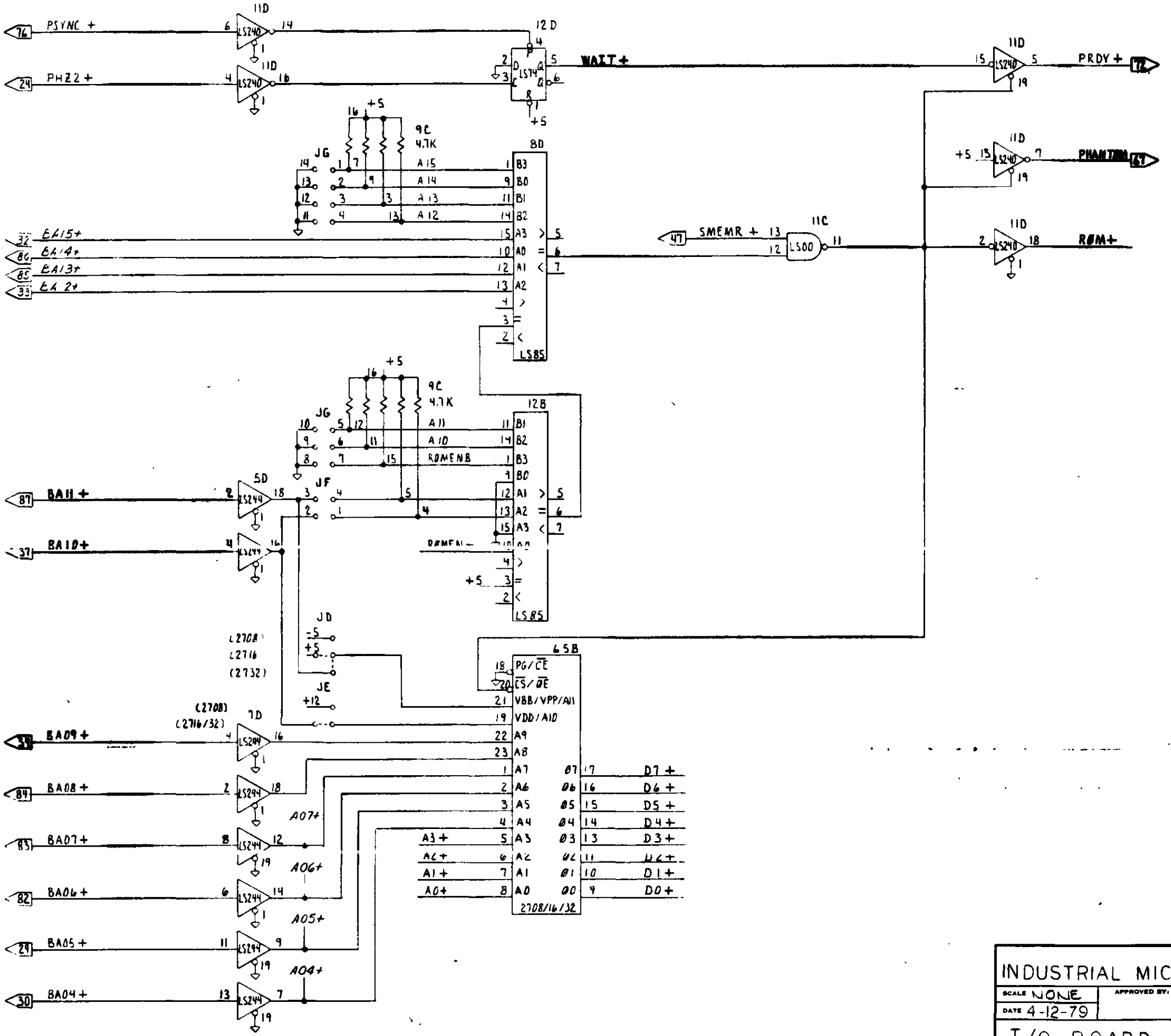
DATE 4-12-79		REVISED JULY 21, 81
I/O BOARD		
L-A00442		DRAWING NUMBER 4 OF 9



INDUSTRIAL MICRO SYSTEMS		
SCALE NONE	APPROVED BY:	DRAWN BY
DATE 4-12-79		REVISED
I/O BOARD		
L-A00442		DRAWING NUMBER 5 OF 9



INDUSTRIAL MICRO SYSTEMS		
SCALE NONE	APPROVED BY	DRAWN BY
DATE 4-12-79		REVISED
I/O BOARD		
L-A00442		DRAWING NUMBER 6 OF 9



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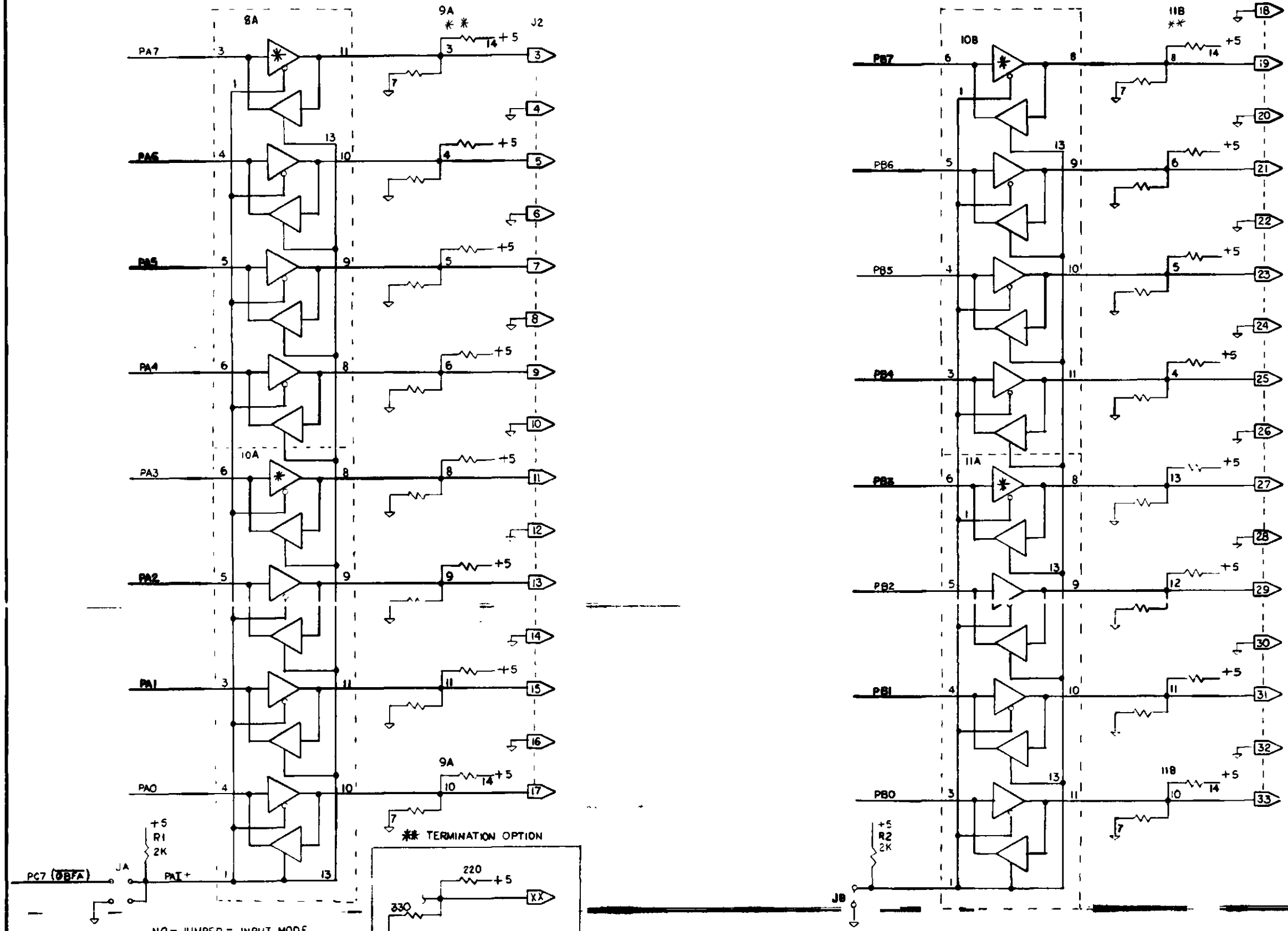
SCALE NONE	APPROVED BY:	DRAWN BY
DATE 4-12-79		REVISED OCT. 6,81
I/O BOARD		
L-A00442		DRAWING NUMBER 7 OF 9

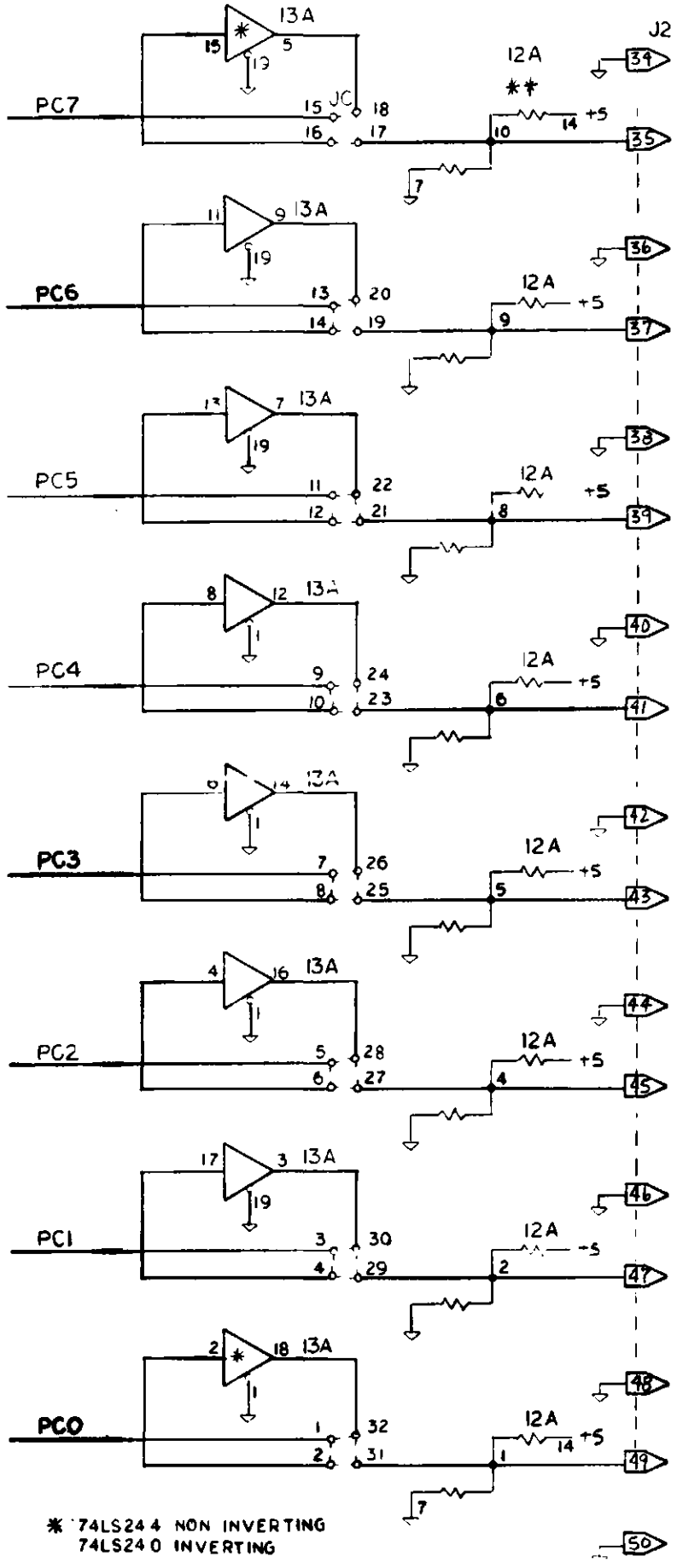


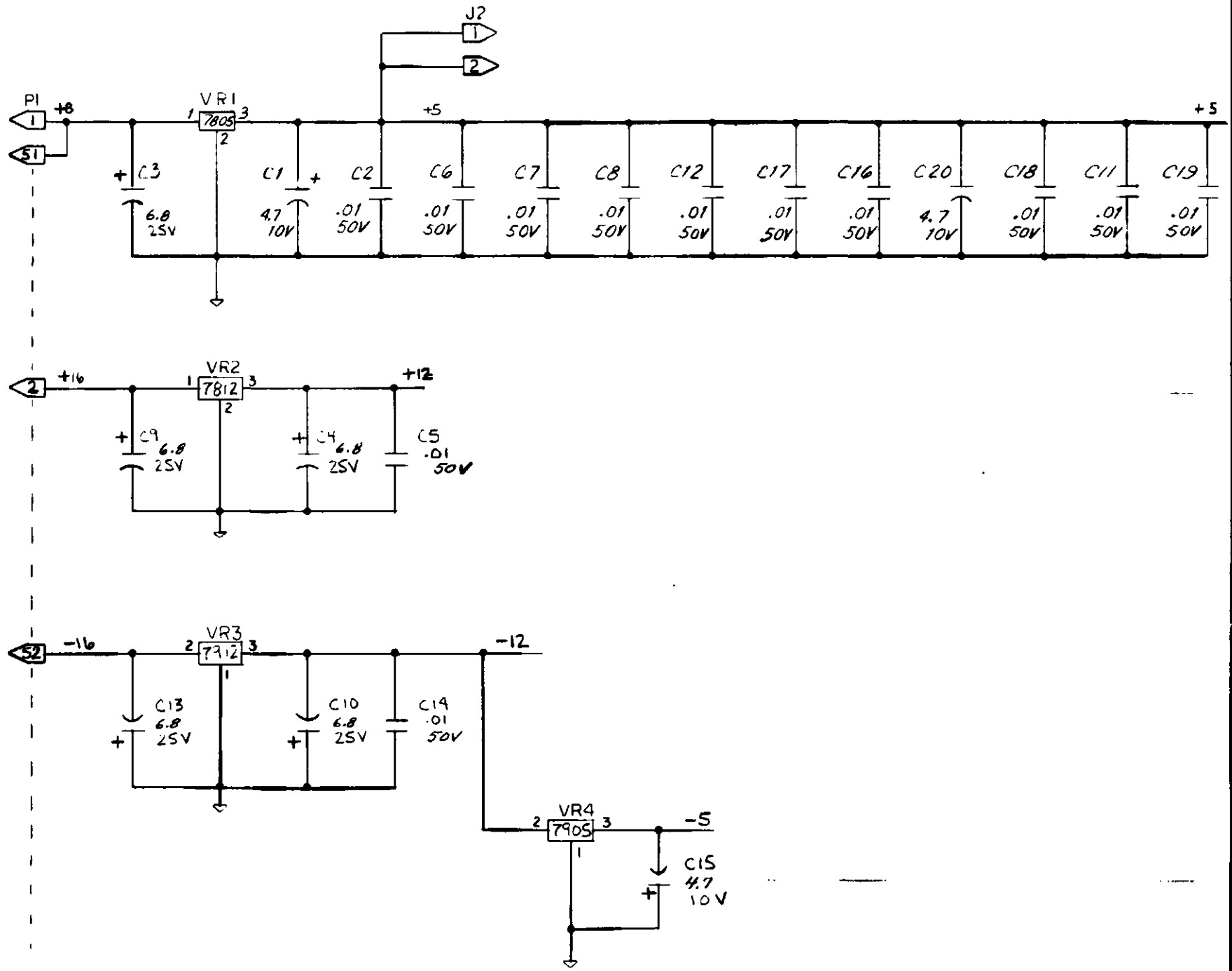
INDUSTRIAL MICRO SYSTEMS

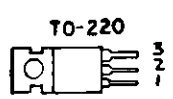
SCALE NONE	APPROVED BY:	DRAWN BY
DATE 4-12-79		REVISED

I/O BOARD

L-A00442 A	DRAWING NUMBER 8 OF 9







INDUSTRIAL MICRO SYSTEMS		
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DATE: 4-12-79		REVISED JULY 23, 81
I/O BOARD		
L-A00442A		DRAWING NUMBER 9 OF 9