INDUSTRIAL MICRO SYSTEMS, INC.

MODEL 464

64K DYNAMIC RANDOM ACCESS MEMORY BOARD

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- 2MHZ OR 4MHZ OPERATION
- PARITY CIRCUITRY
- PHANTOM LINE (PIN 67)
- BANK SELECT LOGIC
- FRONT PANEL COMPATIBLE
- SELECTABLE PORT ADDRESS
- AVAILABLE IN 32K, 48K, OR 64K
- 8080 OR Z80 OPERATION
- HIDDEN REFRESH (M1 CYCLE)
- NO WAIT STATES
- LOW POWER CONSUMPTION

  .6A - +8 VOLTS

  .2A - +16 VOLTS

  .001A - -16 VOLTS

MODELS

GENERAL DESCRIPTION

The Model 464 Dynamic Ram Memory Board is fully buffered and uses 16K X 1 bit dynamic memory circuits. The boards are tested and burned in at 70 degrees centigrade under diagnostic test to insure reliable operations.

The 464 board may be ordered as a 32K, 48K, or 64K memory board. In each of these configurations, the memory is organized into 16K byte banks.

Two modes of operation are provided, Normal Mode and Bank Mode. In the normal mode, the 16K byte banks occupy contiguous address space. In the bank mode of operation, the board is initially disabled and each 16K byte bank may be mapped into selected quadrants of memory (see Bank Selection).

The 464 board provides a "Phantom Line" input for systems with ROM memories which utilize this feature. The user may also configure the board to accept the front panel deposit signal, M-WRITE.

The 464 board features a parity circuit to provide increased data security. A parity bit is written during every memory write such that the total number of "1" bits written are odd. During memory reads the total number of "1" bits are checked. The parity error is set if the number of "1" bits checked are even. Parity errors during memory reads can interrupt or stop the CPU. A LED indicator on the board is lighted to indicate the error. The status of the parity circuit may be read from the memory board's I/O Port.

CONFIGURING THE 464 BOARD

PHANTOM LINE (JACK JD)

The phantom signal (pin 67) shunt is etched so that the board will be disabled by an activated Phantom Line. If this is not desirable, then the etch connecting the two pads of JD (PH) may be cut on the rear of the board.

(JD must be connected when using the 464 board with Industrial Micro System CPU boards.)

Note: The Phantom Line affects memory read operations only. Memory write operations are not affected by the Phantom Line.

EN I/O (JACK JB)

THE "EN I/O" (Enable I/O) shunt JB must be installed for the board to respond to I/O commands. This will be necessary for bank mode or parity operations.

I/O SELECTION (JACK JC)

The selection of the boards I/O address is done on jack JC. The jack is labeled 0-7 (top to bottom) for the respective address bits (A0-A7) of the I/O address. A "1" is programmed by removing a shunt. Thus, to program I/O address 0FH the top four shunts (0-3) would be removed ("1's") and the bottom four shunts (4-7) would be installed ("0's"). (Note that the "EN I/O" shunt must be on for the board to respond to the I/O command.)

CPU SELECTION (JACK JF)

The 8080 shunt (JF) should be installed for systems using 8080 CPU's. For Z-80 systems this shunt should be removed.

FRONT PANEL (JACK JH)

If the 464 board is to be used with an "IMSAI" front panel, the shunt JH must be in the right-most (FP) position.

MEMORY SPEED (JACK JA)

The JA shunt controls the timing of the memory board. The H position is for 200NS RAMS and the L position is for 250NS RAMS. This shunt is factory installed on the H position and normally should not be changed. High speed operation is required for the Z-80 processor.

PARITY INTERRUPT (JACK JG)

Jack JG allows selection of eight different responses to a parity error. The selections are:

SHUNT POSITION	S100 BUS PIN NO.	INTERRUPT SELECTED
VI1	05	VECTORED INTERRUPT 1
VI2	06	VECTORED INTERRUPT 2
VI3	07	VECTORED INTERRUPT 3
VI4	08	VECTORED INTERRUPT 4
VI5	09	VECTORED INTERRUPT 5
INT	73	PINT Line
NMI	12	Non-maskable INT (Z-80 only)
RDY	72	PRDY Line (Parity Error Stops CPU)

When using the parity error circuit, the user must initially write into all memory locations after power is initially applied to condition all the parity bits. After the memory is initialized, the parity error circuit must be reset. The parity error circuit is reset by any output to the I/O port on the memory board. The Power On Clear signal (POC Pin 99 on S100 bus) also resets the parity error circuit.

The state of the parity circuit may be sensed by reading bit "0" of the I/O port on the memory board. A "1" bit indicates a parity error has occurred.

NORMAL/BANK MODE (JACK JE)

The "bank" mode shunt should be installed only if the board is to be used in the Bank Switched mode. In this mode the board will respond to all addresses from 0000 to FFFF hex. For memories that are to be bank selected, this shunt should be installed.

NORMAL MODE

In the normal mode, shunt JE removed, the four 16K memory banks occupy the entire 16 bit address space 0000 thru FFFF hex. In this mode, each 16K bank may be controlled individually by an output to the board's I/0 Port. A "one" bit disables the associated bank. Control is on a bit basis, thus:

OUTPUT DATA	CONTROLLED MEMORY BANK (HEX)	
BIT 0	0000-3FFF	
BIT 1	4000-7FFF	
BIT 2	8000-BFFF	(omitted in 32K version)
BIT 3	C000-FFFF	(omitted in 32K & 48K version)

BANK MODE

In the Bank Mode (Shunt JE installed) the board responds to a combination of bits and bank selection is not done on a bit basis. Codes are provided for a variety of configurations defined in the following table. Initially, the board is deselected by the Power On Clear signal. The 464 memory can be used in a 16K, 32K or 48K bank selection scheme. When the 464 board is ordered in a 48K configuration, Bank 3 is omitted. When ordered in a 32K configuration, Banks 2 and 3 are omitted.

BANK MODE TABLE

OUTPUT DATA	MEMORY MAPPING	
0	All Banks Deselected	
1	Banks 0 & 1 Occupy Addresses	8000-FFFF (32K)
2	Banks 2 & 3 Occupy Addresses	8000-FFFF (32K)
3	Banks 0, 1, & 2 Occupy Addresses	0000-BFFF (48K)
4	Banks 0 & 1 Occupy Addresses	0000-7FFF (32K)
5	Banks 2 & 3 Occupy Addresses	0000-7FFF (32K)
6	Bank 0 Occupies Addresses	C000-FFFF (16K)
7	Bank 0 Occupies Addresses	0000-3FFF (16K)
8	Bank 1 Occupies Addresses	0000-3FFF (16K)
9	Bank 1 Occupies Addresses	C000-FFFF (16K)
A	Bank 2 Occupies Addresses	0000-3FFF (16K)
B	Bank 3 Occupies Addresses	0000-3FFF (16K)
C	Bank 2 Occupies Addresses	C000-FFFF (16K)
D	Bank 3 Occupies Addresses	4000-7FFF (16K)
E	Bank 3 Occupies Addresses	8000-BFFF (16K)
F	Bank 3 Occupies Addresses	C000-FFFF (16K)

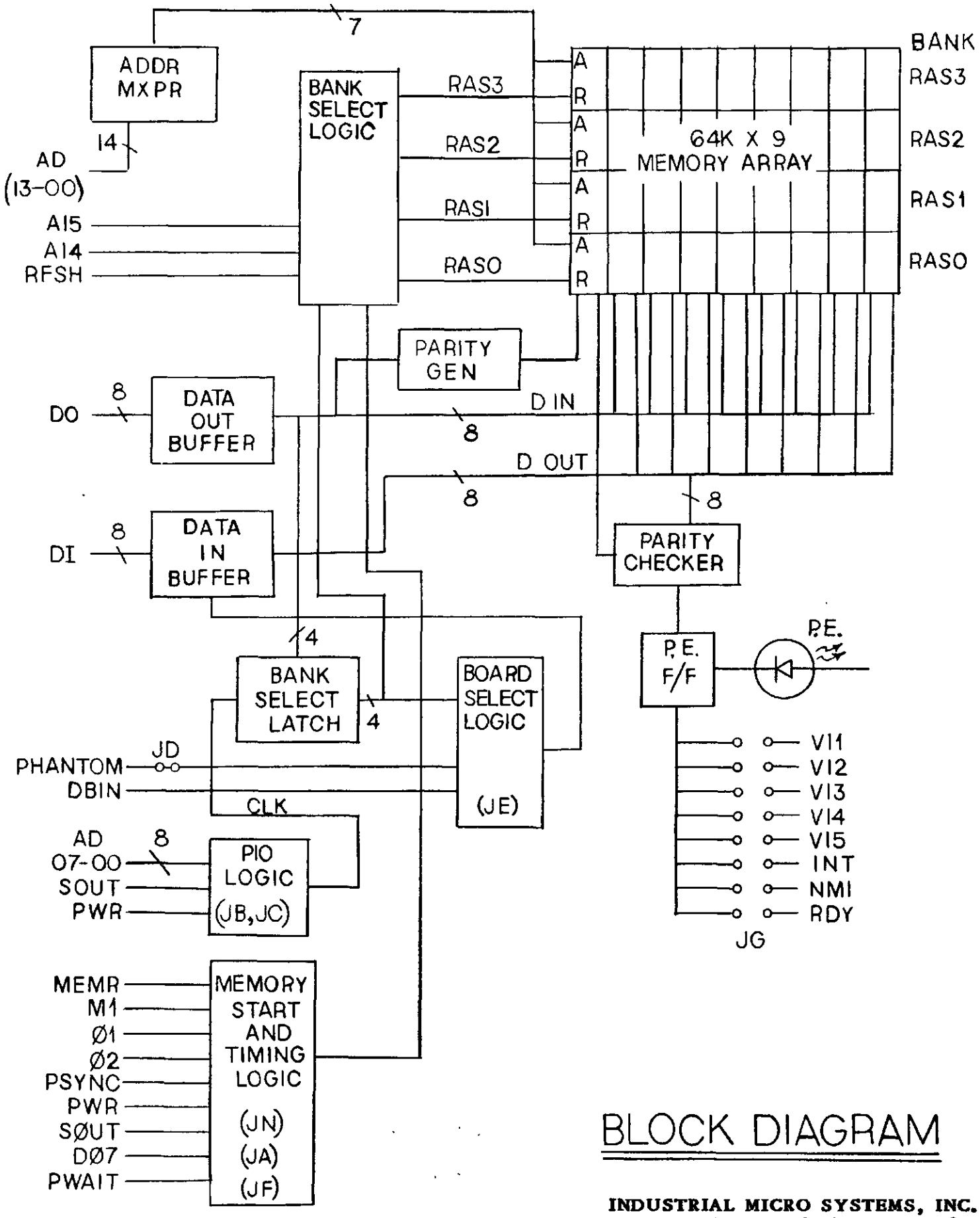
STANDARD CONFIGURATION

IMS supplies the 464 board configured as follows:

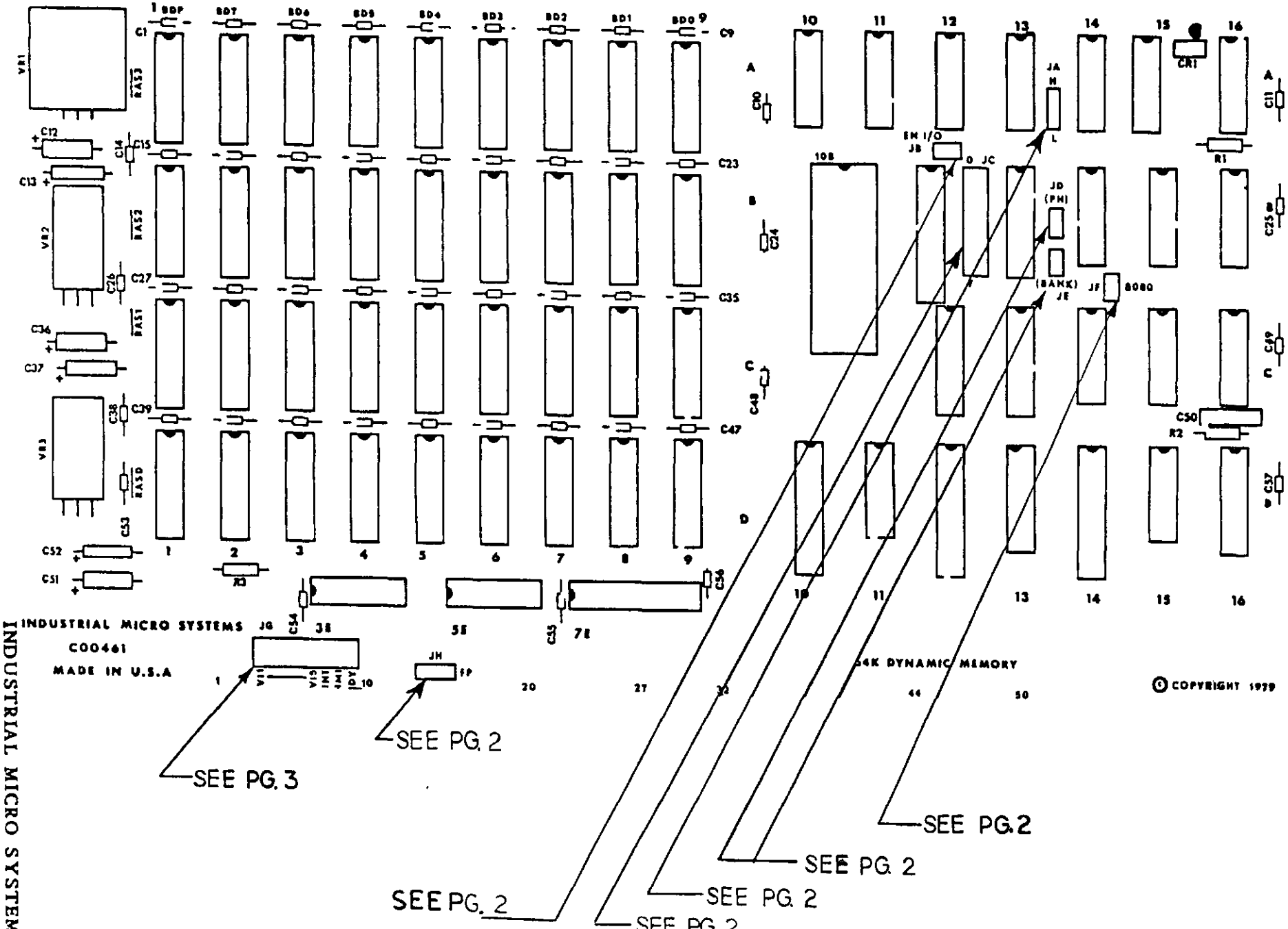
JACK	DESCRIPTION	STANDARD CONFIGURATION
JA	Memory Speed	H Position Shunted
JB	En I/O	Open
JC	I/O Selection	All Positions Shunted
JD	Phantom Line	Shunted (Etch)
JE	Normal/Bank Mode	Open
JF	CPU Selection	Open
JG	Parity Interrupt	All Open
JH	Front Panel	Left Position Shunted

Four spare shunts are installed on the upper pins of Jack G. These pins are all connected by etch and serve as a convenient place to store spare shunts.

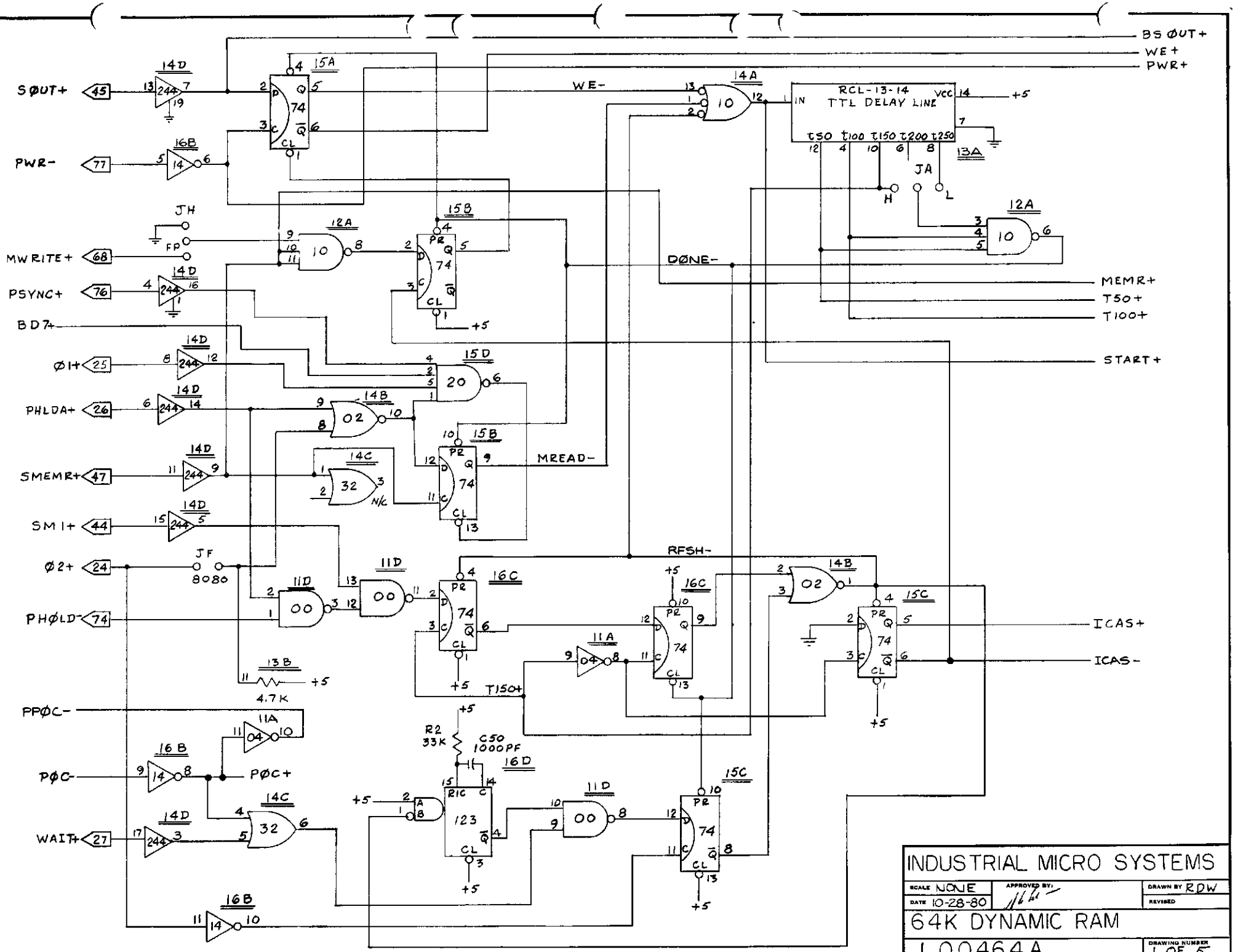
Note: 464 boards shipped in systems will normally be configured to the system requirements.

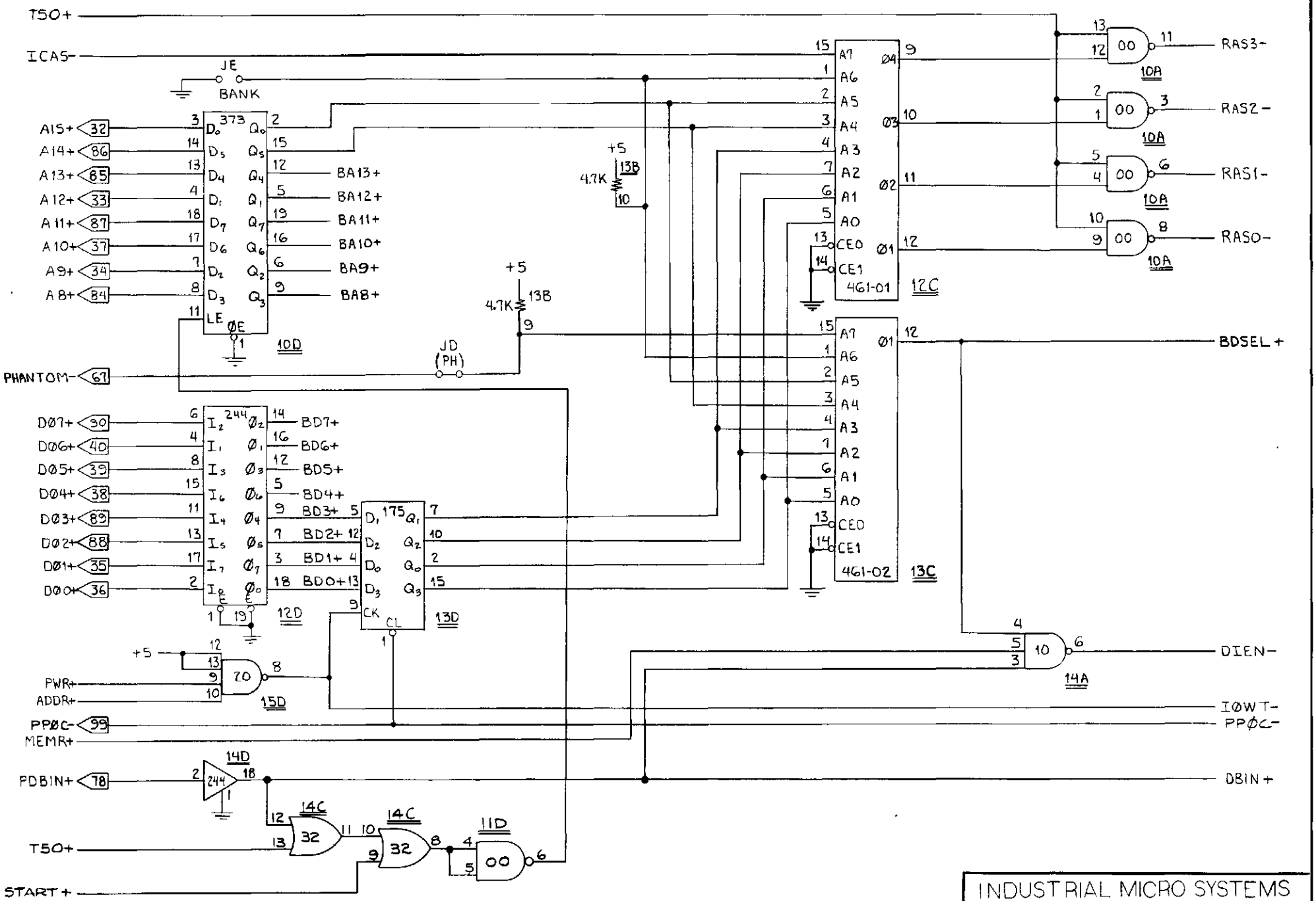


BLOCK DIAGRAM



MODEL 464
STRAPPING OPTION LOCATIONS


BS ØUT+
WE+
PWR+
SØUT+
45
PWR-
77
WE-
RCL-13-14
TTL DELAY LINE
IN
VCC
+5
τ50 τ100 τ150 τ200 τ250
13A
JA
H
L
JH
FP
MWRITE+
68
PSYNC+
76
DØNE-
MEMR+
T50+
T100+
BD7+
START+
Ø1+
25
PHLDA+
26
MREAD-
SMEMR+
47
SM1+
44
Ø2+
24
JF
8080
RFSH-
PHØLD-
74
ICAS+
ICAS-
4.7K
T150+
PPØC-
PØC-
PØC+
R2
33K
C50
1000PF
WAIT+
27
INDUSTRIAL MICRO SYSTEMS
SCALE NONE
APPROVED BY:
DRAWN BY RDW
DATE 10-28-80
REVISED
64K DYNAMIC RAM
L00464A
DRAWING NUMBER
1 OF 5



INDUSTRIAL MICRO SYSTEMS	
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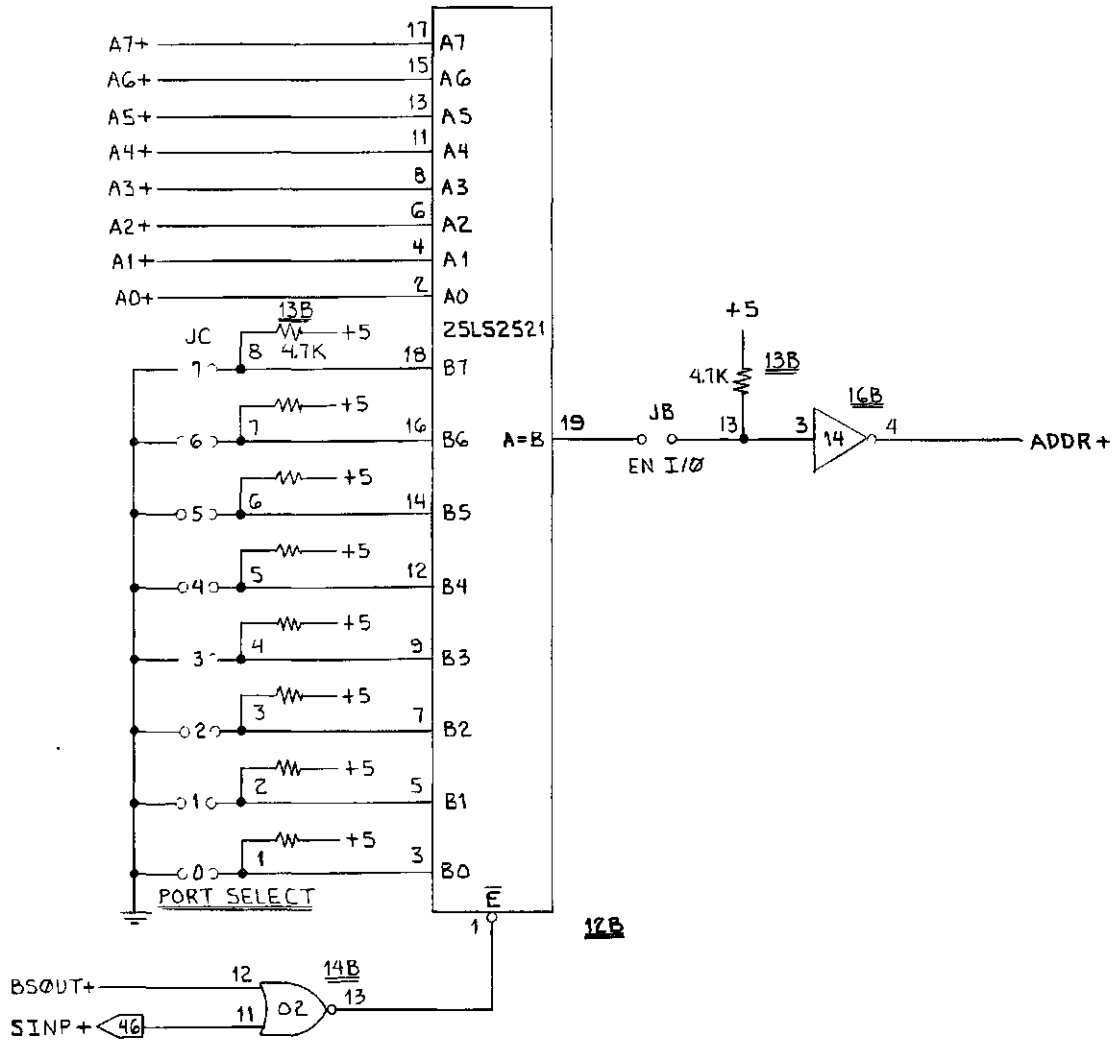
DATE 10-28-80	DRAWN BY RJV
	REVISED
64K DYNAMIC RAM	
L00464A	DRAWING NUMBER 2 OF 5



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64K DYNAMIC RAM	
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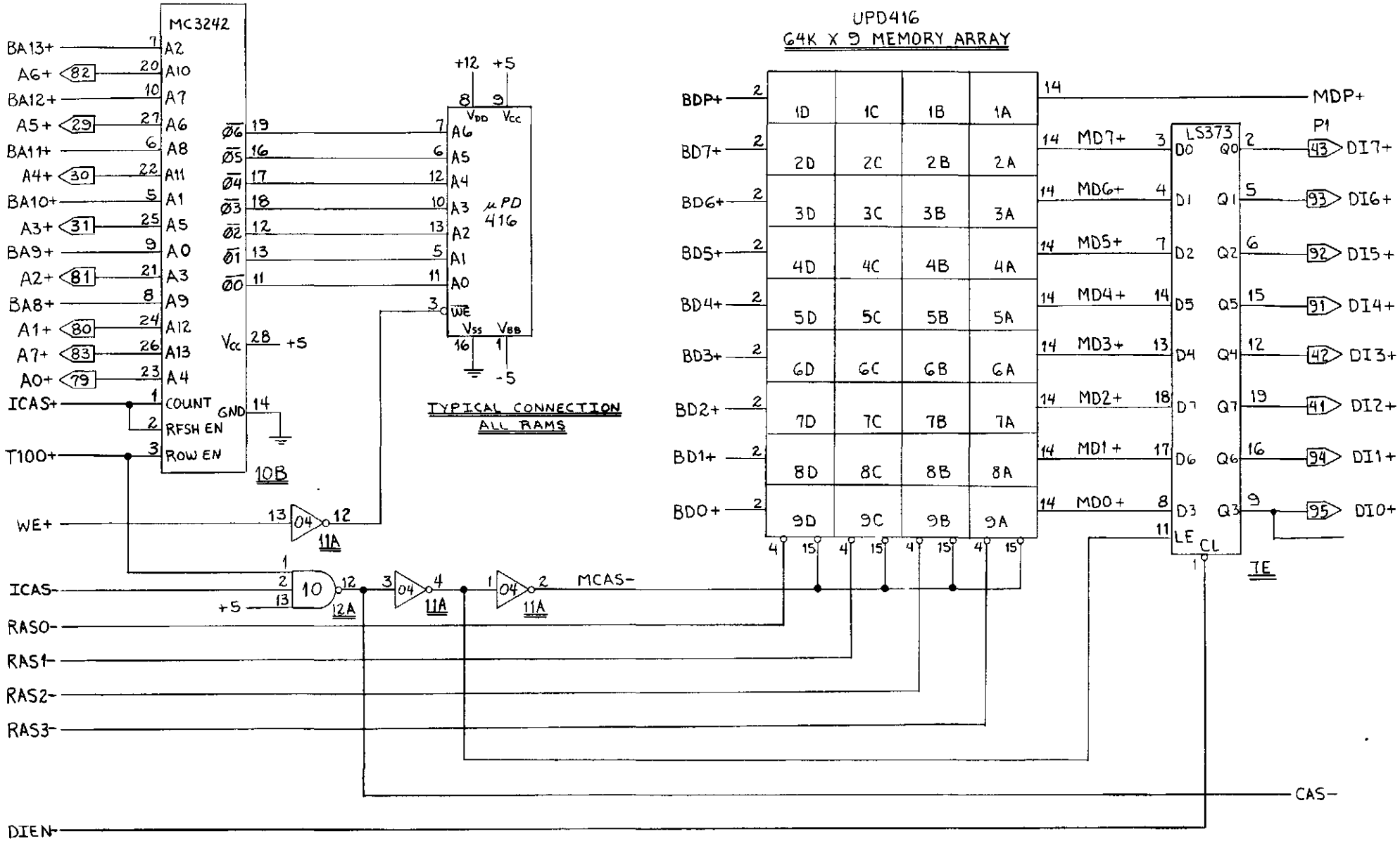

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SCALE NONE	APPROVED BY
DATE 10-28-80	DRAWN BY RJV
	REVISED
64K DYNAMIC RAM	
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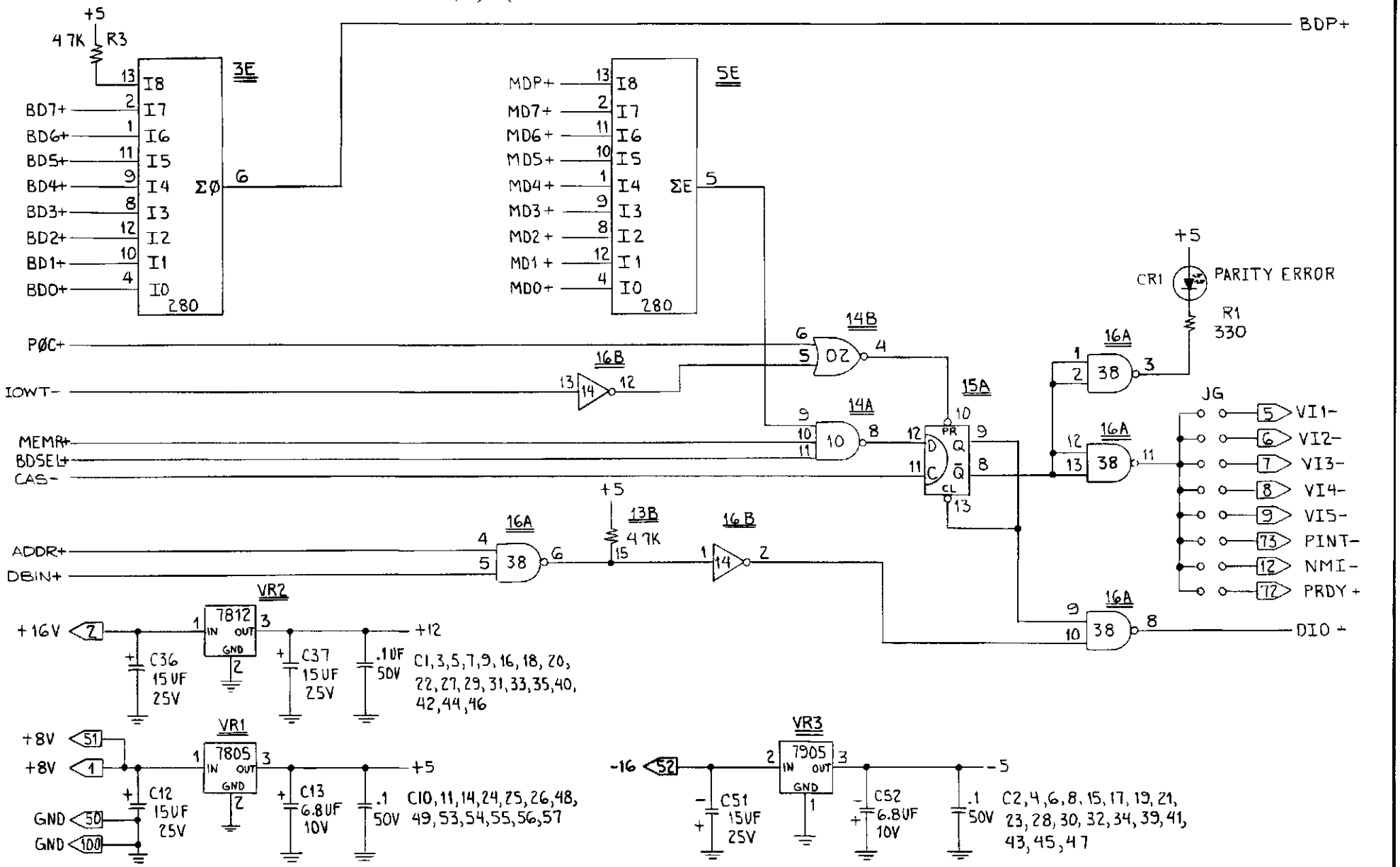

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64K DYNAMIC RAM		
L00464A		DRAWING NUMBER 5 OF 5