MODEL 450 PROCESSOR AND 440 I/O BOARD

GENERAL

The Model 450 & 440 Processor-I/O Boards are the central processing unit of the Industrial Micro Systems Series 5000 and 8000 computer system. The Model 450 provides control and the 440 provides timing, and I/O interfacing for the system.

Control is accomplished by the NEC Z80 LSI (large Scale Integration) microprocessor device. This is a fully parallel, 8-bit, bi-directional, bus oriented processing unit with *a* 16-bit address capability, allowing up to 65 kbytes of directly addressable memory. The Z80 has a 1 usec instruction cycle time.

Timing is provided by the 8253 Programmable Interval Timer (PIT). The PIT is a timer/counter and functions as a general-purpose, multi-mode timing element that generates accurate time delays under software control.

The 6402 Universal Asynchronous Receiver/Transmitter (UART) interfaces the Z80 microprocessor to an asynchronous serial data channel. The UART I converts input serial data to parallel data to be acted upon by the system. Output data is converted from parallel to serial to be placed on the RS-232 PORT.

The 8255 Programmable Peripheral Interface circuit interfaces the Z80 microprocessor to three 8 bit parallel ports. These are located at the 50 pin I/O connector at the top of the 440 card. Each line is TTL buffered and has provision for termination network.

The Model 450 processor consists of a single printed circuit board that nominally occupies the first slot (slot 0) of 12 card slots in the Series 5000 or 8000 computer system. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus system. i

The 450 Processor board consists of the following functional divisions (see Figure 1).

. 8-bit Microprocessor Device (CPU)

. Priority Vectored Interrupt Circuitry

The 440 I/O Board consists of the following functions.

. 1024 by 8-bit Ultraviolet Erasable Programmable Read-only Memory

. Programmable Interval Timer/Real Time Clock

. 2 Universal Asynchronous Receiver/Transmitters (UARTs)

. RS-232 Interface Logic

. 3 eight bit parallel ports

SPECIFICATIONS

. Word Size:	
Address	16 bits
Data	8 bits
. On-board ROM	1 kbyte
. Directly Addressable Memory	64 kbytes
. Clock Frequency	4 MHz
. I/O Ports (Serial)	2
. 8 bit parallel ports	3
. Baud Rate	75 to 9600 baud
. PCB Dimensions	**5.25" x 10"** (13.3 cm x 25.4 cm)
. Power Requirements	440 +16 @ 60 ma + 8 @ 500 ma 16 @ 40 ma 450 + 8 @ 700 ma

Z80 MICROPROCESSOR

The Z80 processor is a bi-directional, bus-oriented, 8-bit parallel LSI device with a 16-bit address capability, allowing up to 64 kbytes of directly addressable memory. The Z80 contains six 8-bit, general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The Z80 has an external stack feature wherein any portion of memory may be used as a last-in/first-out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the six general-purpose registers. The 16-bit stack pointer contains the address of the next available location in the external memory. The program counter is a 16-bit register that contains the program address. The flag register contains six bits of condition code information which indicate the results of the ALU (Arithmetic Logic Unit) operation; Negative (N), Zero (Z), Overflow (V), Carry from Bit 7 (C), and Half-Carry from Bit 3 (H). These are used as testable conditions for the conditional branch instructions. This stack feature allows the ability to provide priority vectored interrupts.

The minimum instruction time for the Z80 microprocessor is 1 usec. Separate 16-bit address and 8-bit bi-directional data lines are used to facilitate easy interface to memory and I/O.

Memory and I/O interface control signals may be used to suspend processor operation and force the address and data lines to a high impedance state (Tri-state allowing Direct Memory Access (DMA) and multi-processor operation.

The Z80 provides 158 variable length instructions (see Z80 instruction set). In addition to performing basic processing functions, the processor is capable of responding to real-time program interrupts, automatic restart in response to the RESET/Power-On RESET signals, and Direct Memory Access operations.

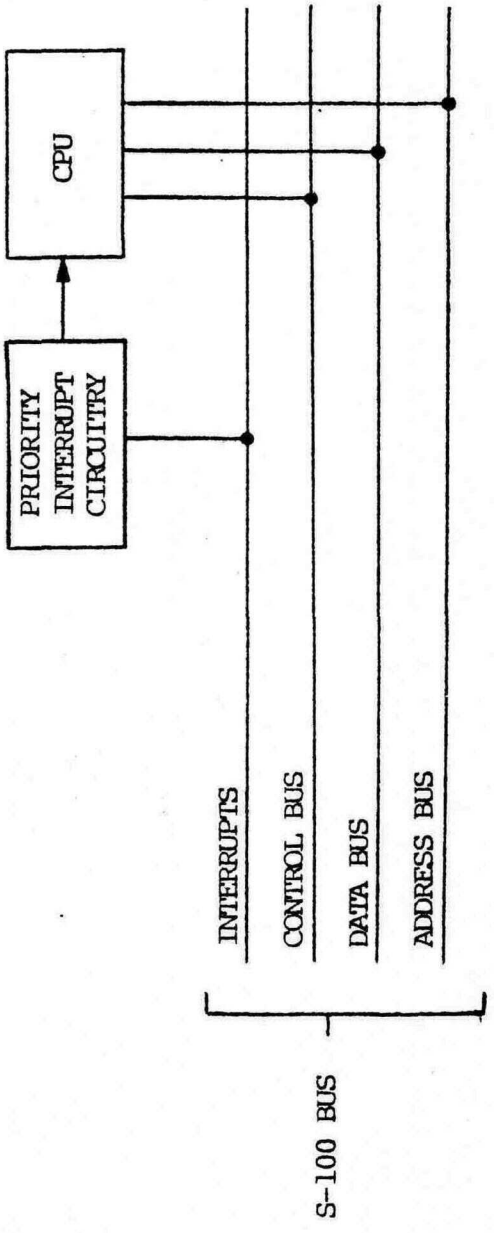


FIGURE 1
Z80 CPU BLOCK DIAGRAM

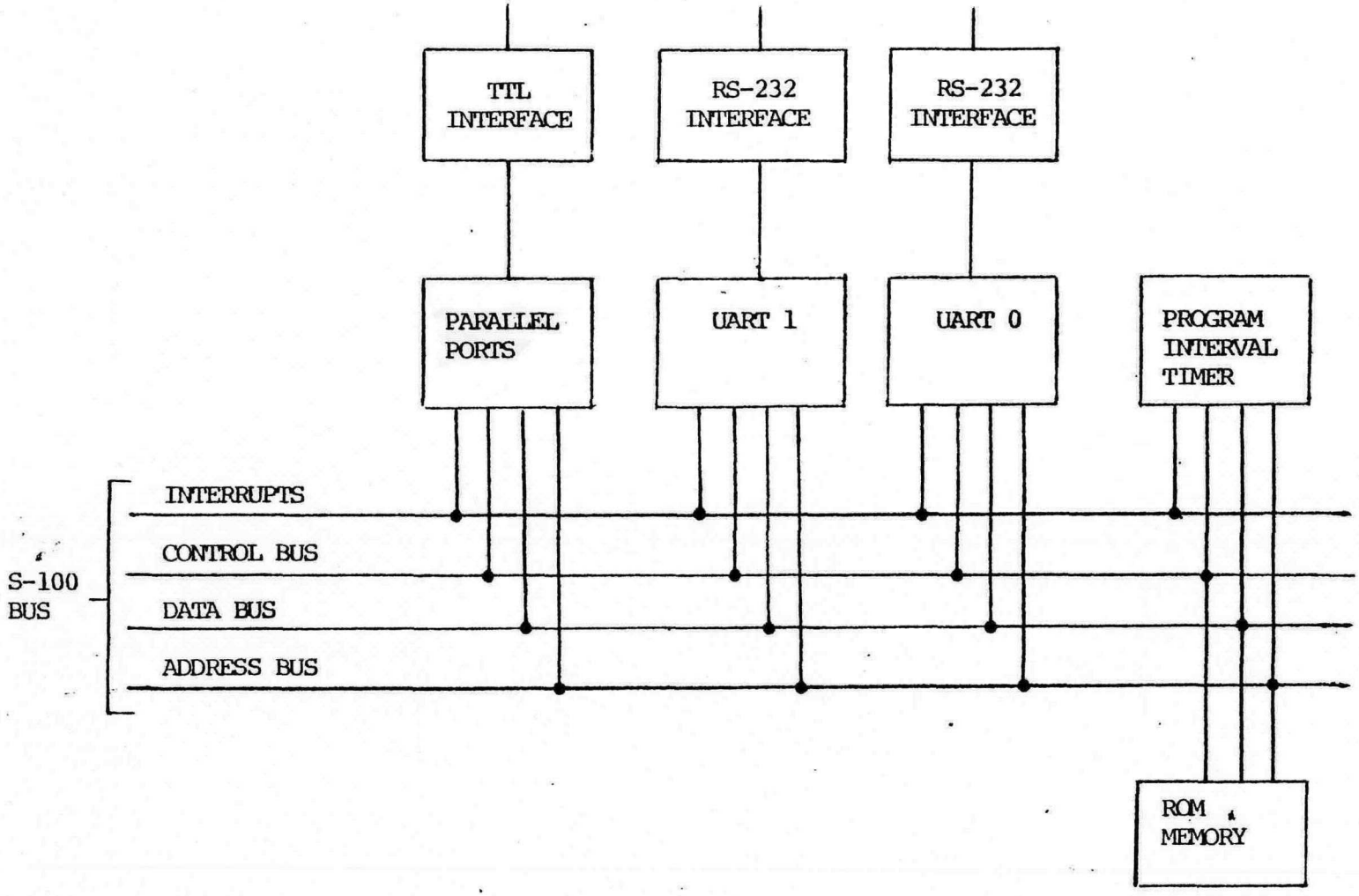


FIGURE 2
440 I/O BOARD BLOCK DIAGRAM

1024 x 8 EPROM (Memory)

The Intel 2708 is a high-speed, bit-erasable, and electrically reprogrammable Read Only Memory (EPROM). It is packaged in a 24-pin, Dual In-line Package (DIP) with a transparent lid, allowing the user to expose the chip to ultraviolet light and erase the bit pattern. A new pattern can then be written into the device. ROM address space is Shunt selectable. The EPROM is used in the 440 Processor to contain the Bootstrap program or a special monitor.

PROGRAMMABLE INTERVAL TIMER

The Intel 8253 Programmable Interval Timer is a programmable counter/timer. Its function is that of a general-purpose, multi-mode timing element that can be treated as an array of I/O ports in the system software.

The 8253 allows the programmer to set up timing loops in the system software so as to generate accurate time delays under software control. The user may initialize one of the three counters with the desired quantity and, upon command, count out the delay and interrupt the CPU when it has completed its tasks. This minimizes software overhead and allows multiple delays that can be easily maintained by assignment of priority levels.

Other counter/timer functions provided by the 8253 are:

- Real Time Clock
- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Digital One-Shot

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The 440 has two on-board serial I/O ports. Each port consists of a 6402 UART. The UART is a programmable MOS/LSI device used for interfacing an asynchronous serial communication line to the parallel data lines of the microprocessor.

The UART is made up of two separate and independent sections:

1. The receiver
2. The transmitter

RECEIVER

The receiver accepts the serial data, converts it to parallel and decodes it. The decode function converts the serial Start, Data, Parity, and Stop bits to parallel information and verifies the proper code transmission by checking parity and the receipt of a valid stop bit.

TRANSMITTER

The transmitter section converts the parallel data into a serial word which contains the data, along with the start, parity, and stop bits.

Both the receiver and transmitter are double-buffered. The UART may be programmed as follows:

1. The word length may be either 5, 6, 7, or 8 bits.
2. Parity generation and checking may be inhibited, and the parity may be odd or even.
3. The number of stop bits may be one or two (1.5 when transmitting a 5-bit code).
4. The baud rate may be set from 75 to 9600 baud.

RS-232C VOLTAGE INTERFACE

The two serial ports of the 340 processor go to the system peripherals through industry standard EIA RS-232C voltage interfaces.

HARDWIRE SUMMARY

The instruction set of the 450 is that of the Z80 microprocessor device. The processor has a 1 usec instruction cycle time, the ability to provide priority vectored interrupts, and the capacity for 256 bi-directional I/O ports.

FUNCTIONAL OVERVIEW (See Figure 1)

The S-100 bus interface consists of three separate sets of lines:
1) address lines, 2) data lines, and 3) control lines..

ADDRESS – The 16 address lines (A0-A15) allow each of 65,536 bytes of memory to be uniquely addressed.

The address lines are utilized by either the microprocessor or a direct memory access (DMA) device, such as the disk controller. These lines are decoded by each memory module so that only one memory location is addressed by an exclusive bit pattern.

DATA – The data lines are further sectioned into two sets of lines:
1) input data, and 2) output data.

The input data lines (DI0-DI7) carry the binary data in parallel from the memory to the 450 processor.

The output lines (DO0-D07) carry the binary data in parallel from the 450 processor to memory.

CONTROL – The remaining bus lines perform various control functions:
1) timing, 2) synchronization, 3) data direction and 4) status.

TIMING and SYNCHRONIZATION — These control lines are:

0 CLOCK	PSYNC
0 CLOCK	READY1
CLOCK-	READY2
SMI	WAIT

01 and 02 (phase 1 and phase 2) clocks, along with CLOCK-, are generated by the microprocessor clock circuit and are the main timing signals.

PSYNC, XRDY, and SYNC enable and initialize the clock circuit. The 16 MHz crystal provides the base frequency for the oscillator. From this circuit 02 clock is used by the microprocessor for control timing.

STATUS — The status signals and the corresponding data bits are as follows:

BIT	STATUS TERM
DO	SMEMR+
Dl	SINP+
D2	SMl+
D3	SOUT+
D4	SHLTA+
D5	
D6	SWO—
D7	SINTA+

The eight status lines are placed on the bus by the microprocessor to be selectively used by the memory and I/O boards to obtain information as to the nature of the cycle.

INTERRUPTS – The vectored priority interrupt system consists of eight interrupt lines as follows:

INTERRUPTS	DESCRIPTION
VIO-VI5	User defined
V^^BMk	Communication interrupt V7 RTC interrupt
V7	RTC interrupt

The interrupts[1] function is to indicate to the CPU that there are peripheral devices that need to be serviced. When the priority requirements are fulfilled, the CPU goes into the Interrupt Service Routine and responds to the device requesting the interrupt.

PORT CONTROL.——Port\X8H interrupt mask, request——t6——s

assignments are as follows:

BIT	DESCRIPTION
0	ROM disabled = 1
1	Real Time Clock interrupt enable = 1
2	UART 1 transmit interrupt enable = 1
3	UART 1 receive interrupt enable = 1
4	UART 1 request-to-send
5	JJART 0 transmit interrupt enable = 1
6	UART 0 receive interrupt enable = 1
7	UART 0 request-to-send

The Real Time Clock (RTC) interrupt (bit 1) is reset when out X9H is executed.

The ROM Enable/Disable (bit 0) shunt is located on JG 7-8.

UART CONTROL – Control for UART 0 is accomplished by the following line and bit assignments:

BIT	FUNCTION
Out X0H= Control	
0	Parity inhibit
1	Even parity enable
2	Stop bit select -
3	Word length - LSB
4	Word length - MSB
Out X1H = Transmitted data out	
In X0H = Status	
0	Receive data ready
1	Transmit holding register empty
2	Parity error
3	Framing error
4	Overrun error
7	Clear-to-send
In X1H = Received data in	

Line and bit assignments for UART 1 are as follows:

Out X2H= Control

Out X3H= Transmitted data out

In X2H = Status

In X3H = Receive data in

(Bit assignments are the same as UART 0)

PIT CONTROL – The Programmable Interval Timer provides three independent counters for interrupt timing:

Counter 0	UART 0 Clock
Counter 1	UART 1 Clock
Counter 2	Real Time Clock

Output X7H provides control for the PIT. An output to line (port) X7H must be accomplished before establishing the timing intervals for each counter. The division factor is loaded into each count register to establish the desired frequency output. The base clock frequency is 2MHz. The following values should be output to port X7H for each counter, as follows:

COUNTER	OUTPUT
0	36H
1	76H
2	B6H

To load the count registers, the desired division rate should be output (least significant byte first) for the counters as follows:

COUNTER	OUTPUT
0	Port X4H
1	Port X5H
2	Port X6H

The algorithm for determining the baud rate for the UARTS is as follows, using baud 9600 for the example:

$$\text{Input frequency} = \frac{2{,}000{,}000}{\text{baud} \times 16} = \frac{2{,}000{,}000}{9600 \times 16} \sim 13_{10} = 000DH$$

Note that the UART requires an input frequency of 16 times the baud rate.

So: 1. Output 36H to port X7, then

2. Output ODH to port X4, then

3. Output OOH to port X4

The UART is now set to run at 9600 baud.

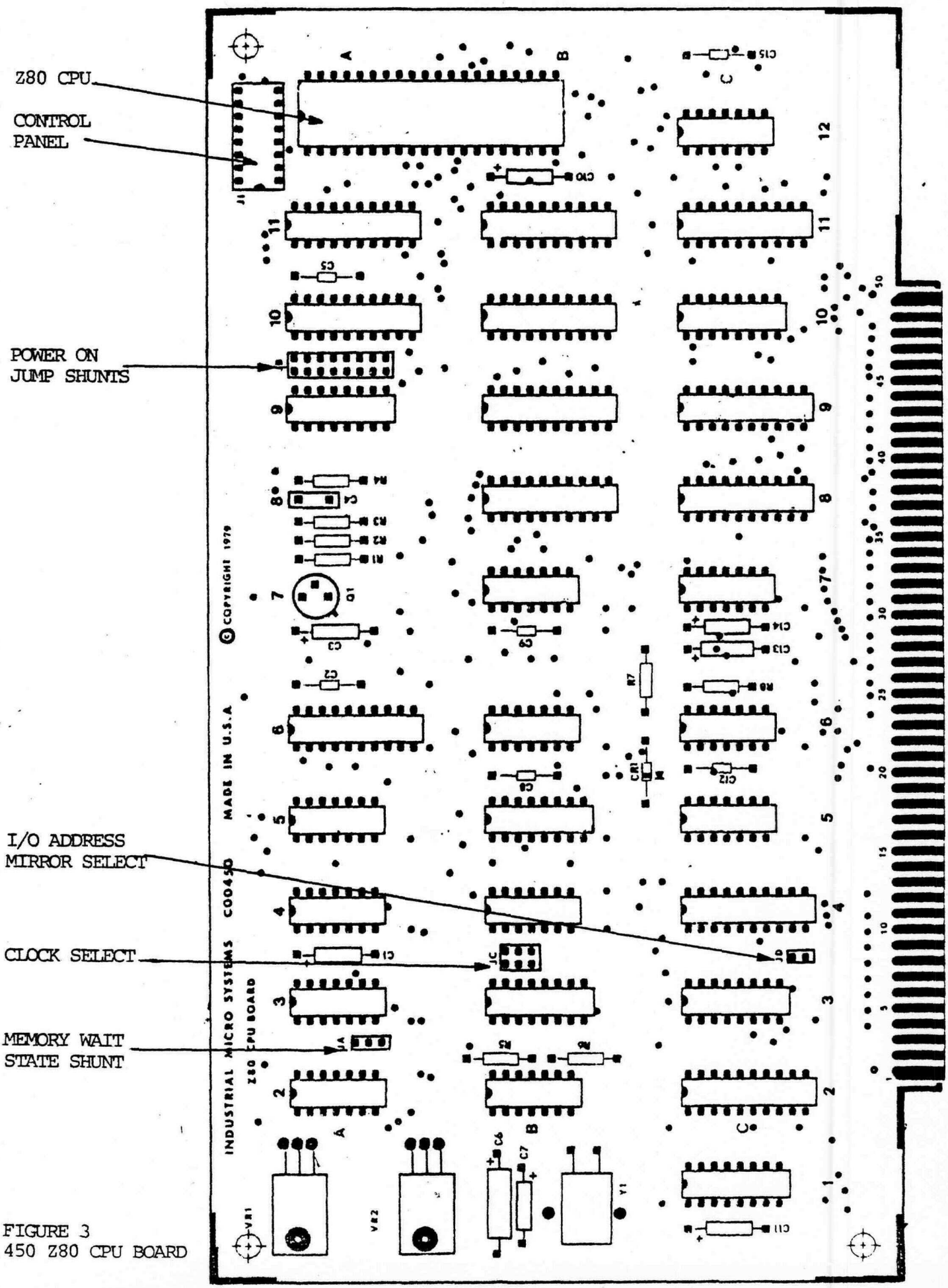
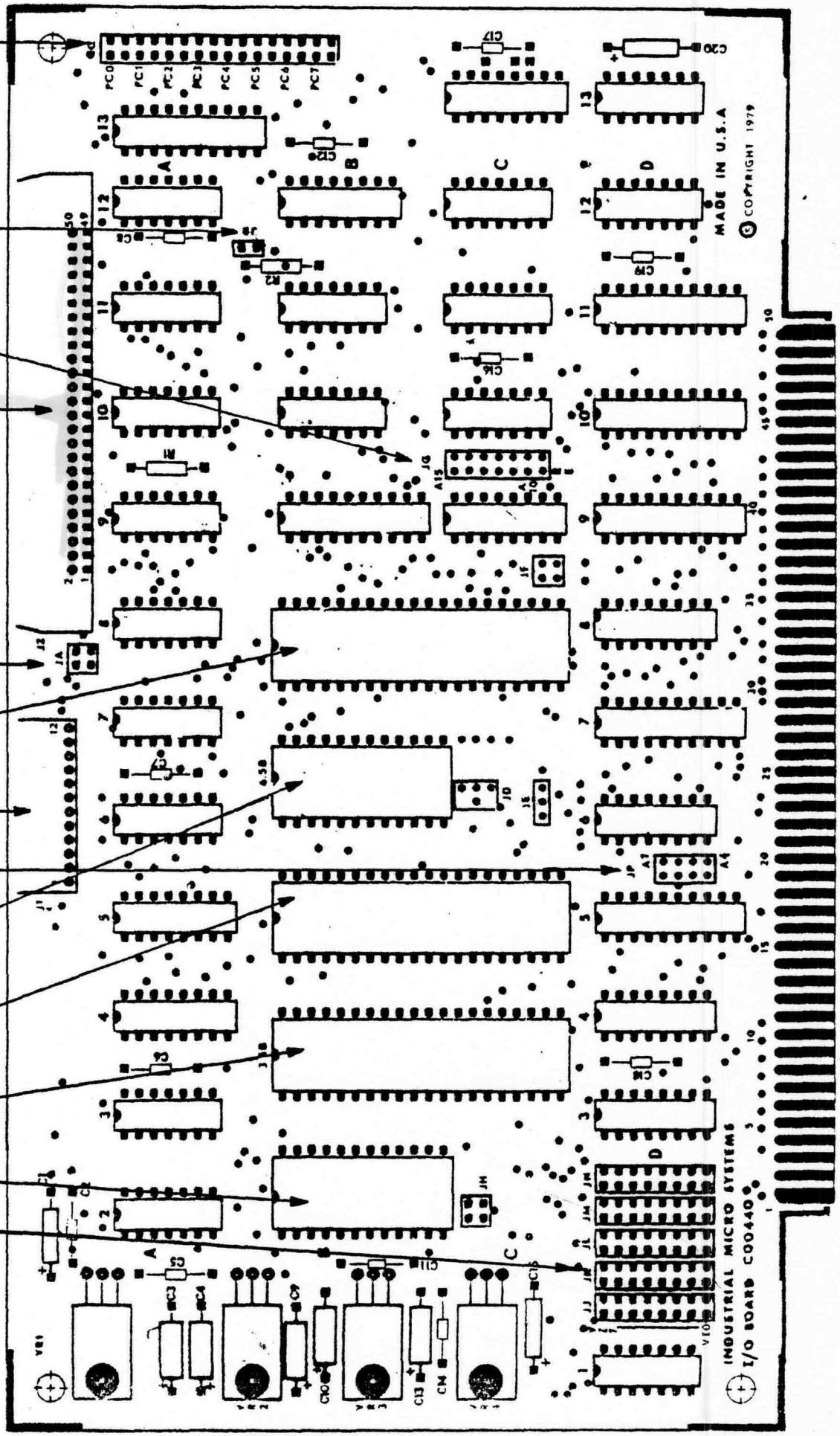


FIGURE 3
450 Z80 CPU BOARD

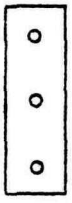


URE 4
440 I/O BOARD

MODEL 450 Z80 CPU BOARD

SHUNT AND JUMPER OPTIONS

JA



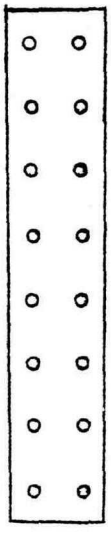
WAIT STATE SELECT LOC. 2.5A

No Shunts = No Memory Wait State

Shunt JA 1-2 = Provides One Wait State

Shunt JA 2-3 = Provides Two Wait States

JB



1	16	A15
2	15	A14
3	14	A13
4	13	A12
5	12	A11
6	11	A10
7	10	A 9
8	9	A 8

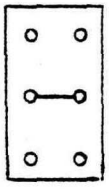
POWER ON ADDRESS SELECT LOC. 9.5A

Shunt Off = 1 Shunt On = 0

(All Shunts Off Power On Address = $FF00_{16}$)

(All Shunts On Power On Address = 0000_{16})

JC

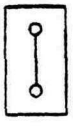


1	6	
2	5	4MHZ
3	4	2MHZ

CPU CLOCK SELECT: LOC. 3.5B

Cut Etch Jumper to Change CPU Clock

JD



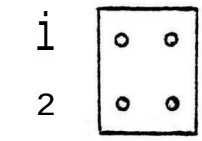
ADDRESS MIRROR SELECT LOC. 3.5C

Cut Etch Jumper for No Address Mirror

MODEL 440 I/O BOARD

SHUNT AND JUMPER OPTIONS

JA



PARALLEL PORT A SELECT LOC. 7.5A

No Shunts = Input Mode
Shunt JA 1-4 = Output Mode
Shunt JA 2-3 = Bidirectional Mode

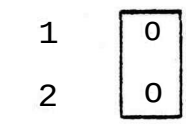
PORT A DRIVER/RECEIVER LOC. 8A, 10A

74LS243 Non Inverting
74LS242 Inverting

PORT A TERMINATION OPTIONS LOC. 9A

Open No Termination
Beckman S99-1-R1.0K 1K Pull Up Termination
Beckman 899-5-R2201330 2201330 Pull Up/Pull Down Termination

JB



PARALLEL PORT, PORT B SELECT LOC 11.5B

No Shunt - Input Mode
Shunt JB 1-2 = Output Mode

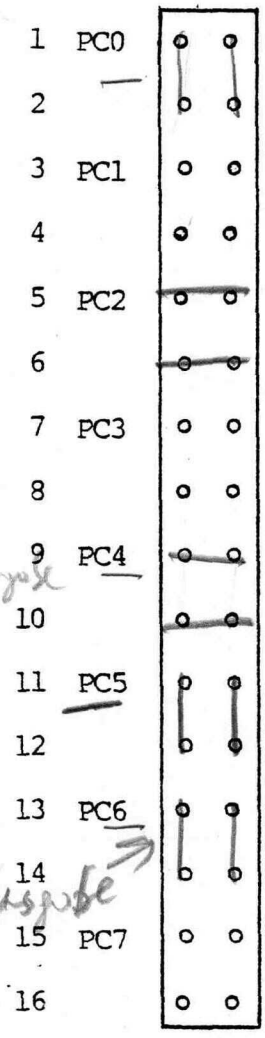
PORT B DRIVER/RECEIVER LOC. 10B, 11A

74LS243 Non Inverting
74LS242 Inverting

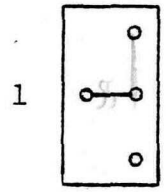
PORT B TERMINATION OPTION LOC. 11B

Open No Termination
Beckman 899-1-Rl.0K 1K Pull Up Termination
Beckman 899-5-R2201330 2201330 Pull Up/Pull Down Termination

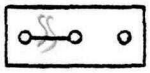
JC



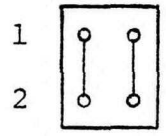
JD



JE

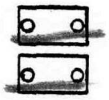


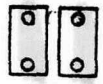
JF



PARALLEL PORT C SELECT LOC. 13.5A

No Shunts = Bit Unused

Shunts = PCX  Input Receiver

Shunts = PCX  Output Driver

PORT C DRIVER/RECEIVER LOC. 13A

74LS244 Nan Inverting

74LS240 Inverting

PORT C TERMINATION OPTION LOC. 12A

Open No Termination

1K Pull Up Termination

2201330 Pull Up/Pull Down Termination

Note: For more detail regarding the programming of the 8255A see the INTEL Peripheral Design Handbook.

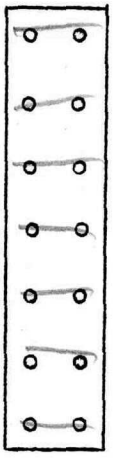
ROM SELECT LOC. 6.5B

2708 1K X 8 Etch Jumper JD 1-3 VBB = -5
JE 1-2 VDD = +12
JF 1-2 A10
JF 3-4 All

2716 2K X 8 Cut Etch Jumper
JD 1-3 Add JD 3-4 +5
JE 1-2 JE 2-3 A10
JF 3-4

2732 4K X 8 Cut Etch Jumper
JD 1-3 Add JD 2-3 All
JE 1-2 JE 2-3 A10
JF 1-2
JF 3-4

JG

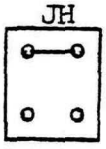


1	A15		14
2	A14		13
3	A13		12
4	A12		11
5	A11		10
6	A10		9
7	RE		8

ROM ADDRESS SELECT LOC. 9.5C

Shunt Off = 1 Shunt On = 0
(All Shunts Off = ROM Starting Address $FC00_{16}$)
(All Shunts On = RDM Starting Address 0000_{16})

JH



	1		4
	2		3

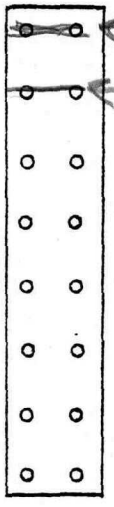
RE-ROM ENABLE

Shunt Off ROM Disabled, Shunt on ROM Enabled

TIMER CLOCK OPTION LOC. 2C Etch Jumper JH1-4 ;=External 2MHZ

Etch Jumper JH 1-4 = External 2MHZ
Cut Etch Jumper JH 1-4 Add Jumper JH 2-3
Add OSC at LSD and 74LS161 at 13C
For Internal Timer Clock

JJ-JN



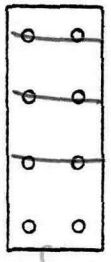
1	VI7		16
2	VI6		15
3	VI5		14
4	VI4		13
5	V13		12
6	V12		11
7	VI1		10
8	VI0		9

INTERRUPT OPTIONS LOC. 2D, 3D

The installing of a shunt will attach the selected interrupt level to the function as defined below:

JJ - Real Time Clock Interrupt
JK - Line 0 Transmit/Receive Interrupt
JL - Line 1 Transmit/Receive Interrupt
JM - Parallel Port B Interrupt (PCD $INTR_B$)
JN - Parallel Port A Interrupt (PC3 $INTR_A$)

JP



1	A 7		8
2	A 6		7
3	A 5		6
4	A 4		5

I/O DEVICE ADDRESS SELECT LOC. 5.5D

Shunt Off = 1 Shunt On = 0
(All Shunts Off = I/O Address F0 - FF_{16})
(All Shunts On = I/O Address 00 - $0F_{16}$)

I/O DEVICE ADDRESS

X0	COMM 0 R/W CTRL	)
		)
XI	COMM 0 R/W DATA	)
		)— 6402
X2	COMM 1 R/W CTRL	)
		)
X3	COMW 1 R/W DATA	)
X4	TIMER 0 R/W DATA (BAUD CLOCK X 16 COMM 0	)
		)
X5	TIMER 1 R/W DATA (BAUD CLOCK X 16 COMM 1	)— 8253
		)
X6	TIMER 2 R/W DATA (RTC)	)
X7	TIMER CONTROL WRITE	
X8	INTERRUPT ENABLE / REQUEST TO SEND CTRL	
X9	TIMER 2 INTERRUPT RESET (RTC)	
XA		
XB		
XC	PARALLEL PORT A R/W DATA	)
		)
XD	PARALLEL PORT B R/W DATA	)
		)— 8255
XE	PARALLEL PORT C R/W DATA	)
		)
XF	PARALLEL CONTROL WRITE	)

X = SHUNT SELECTED

= X'10 I

MODEL 440 I/O BOARD

PARALLEL PORT CONNECTOR PIN LISTING

1.	+5VDC	2.	+5VDC
3.	PA7	4.	GND
5.	PA6	6.	GND
7.	PA5	8.	GND
9.	PA4	10.	GND
11.	PA3	12.	GND
13.	PA2	14.	GND
15..	PA1	16.	GND
17.	PA0	18.	GND
19.	PB7	20.	GND
21.	PB6	22.	GND
23.	PB5	24.	GND
25.	PB4	26.	GND
27.	PB3	28.	GND
29.	PB2	30.	GND
31.	PBl	32.	GND
33.	PB0	34.	GND
35.	PC7	36.	GND
37.	PCS	38.	GND
39.	PC5	40.	GND
41.	PC4	42.	GND
43.	PC3	44.	GND
45.	PC2	46.	GND
47.	PC1	48.	GND
49.	PCD0	50.	GND

PAX	PARALLEL	PORT A	BITS
PBX	PARALLEL	PORT B	BITS
PCX	PARALLEL	PORT C	BITS

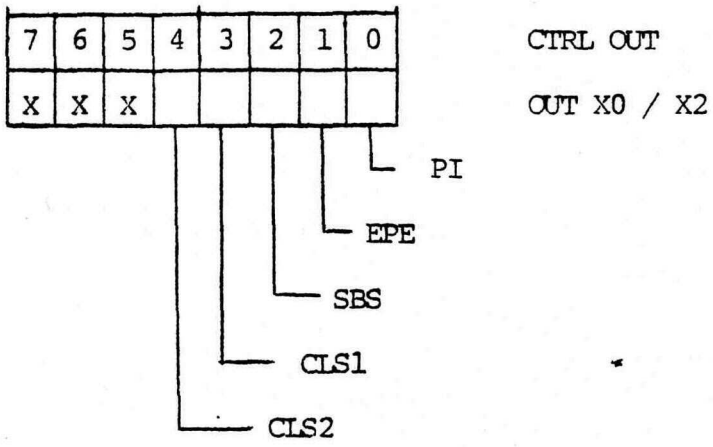
STANDARD ASSIGNMENTS

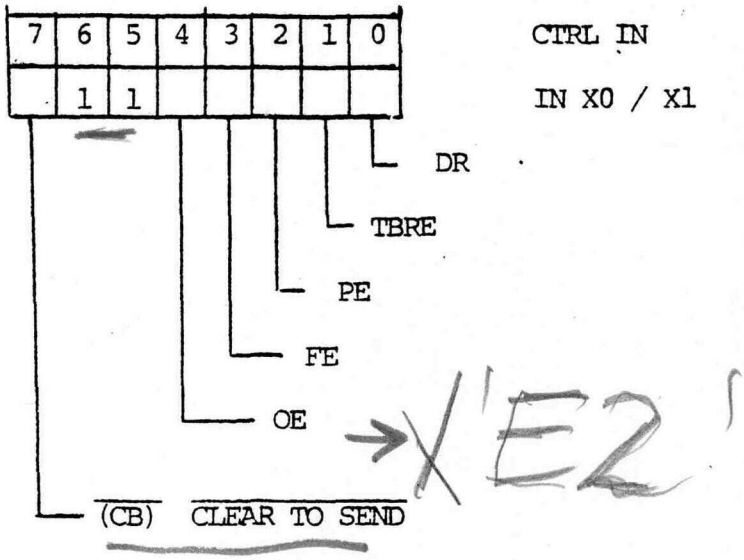
INTERRUPTS

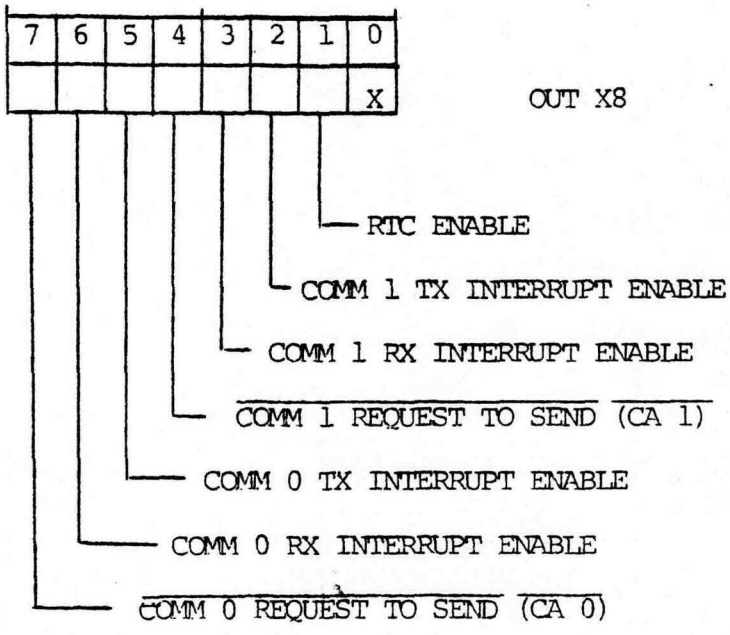
VI0	00	POWER ON
VI1	08	
VI2	10	
VI3	18	PRINTER
VI4	20	EXTERNAL COMMUNICATION
VI5	28	EXTERNAL RTC
VI6	30	COMMUNICATION
VI7	38	RTC

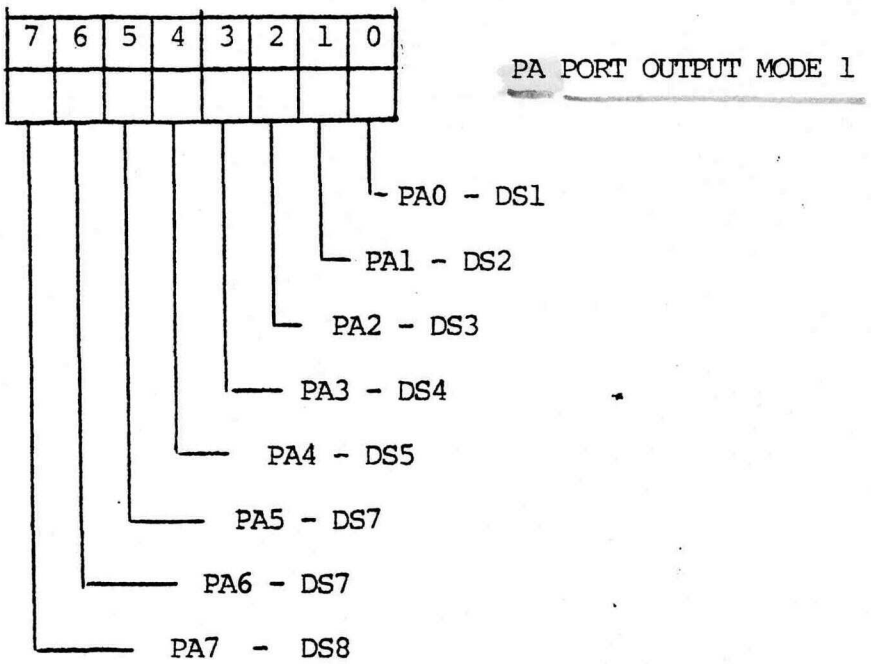
I/O DEVICE ADDRESS

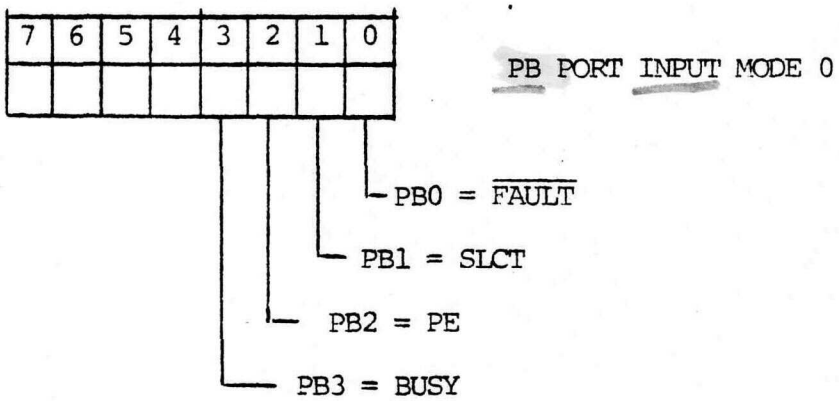
10	COMM 0	R/W CTRL
11	COMM 0	R/W DATA
12	COMM 1	R/W CTRL
13	COMM 1	R/W DATA
14	TIMER 0	R/W
15	TIMER 1	R/W
16	TIMER 2	R/W
17	TIMER CTRL	
18	INTERRUPT MASK / CA CTRL	

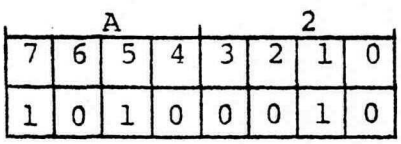

7 6 5 4 3 2 1 0
X X X
CTRL OUT
OUT X0 / X2
PI
EPE
SBS
CLS1
CLS2


7 6 5 4 3 2 1 0
1 1
CTRL IN
IN X0 / X1
DR
TBRE
PE
FE
OE
(CB) CLEAR TO SEND


7 6 5 4 3 2 1 0
X
OUT X8
RTC ENABLE
COMM 1 TX INTERRUPT ENABLE
COMM 1 RX INTERRUPT ENABLE
COMM 1 REQUEST TO SEND (CA 1)
COMM 0 TX INTERRUPT ENABLE
COMM 0 RX INTERRUPT ENABLE
COMM 0 REQUEST TO SEND (CA 0)

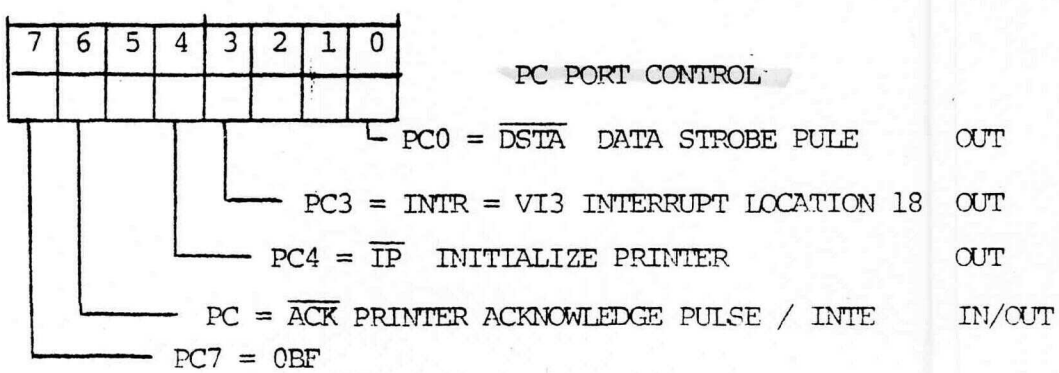






CONTROL WORD

PORT A OUTPUT MODE 1
PORT B INPUT MODE 0
PORT C UPPER OUTPUT
PORT C LOWER OUTPUT



PCX BIT SET/RESET FORMAT FOR CENTRONICS PRINTER

	0				0			
7	6	5	4	3	2	1	0	CONTROL DEVICE ADDRESS XF
0	X	X	X	0	0	0	0	RESET PC0 $\overline{\text{DSTA}}$
	0				1			
0	X	X	X	0	0	0	1	SET PC0 $\overline{\text{DSTA}}$
	0				8			
0	X	X	X	1	0	0	0	RESET PC4 $\overline{\text{IP}}$
	0				9			
0	X	X	X	1	0	0	1	SET PC4 $\overline{\text{IP}}$
	0				C			
0	X	X	X	1	1	0	0	RESET PC6 INTE
	0				D			
0	X	X	X	1	1	0	1	SET PC6 INTE

PCX SHUNTS FOR CENTRONICS PRINTER

1. SHUNT PC3 (INTR) TO INTERRUPT VI3 LOCATION 18 JN 5-12
2. SHUNT PAI TO GND SO PAX = OUTPUT JA 1-4
3. INSTALL 74LS244 FOR PC DRIVER
4. SHUNT PCO JC 1-2 DSTA

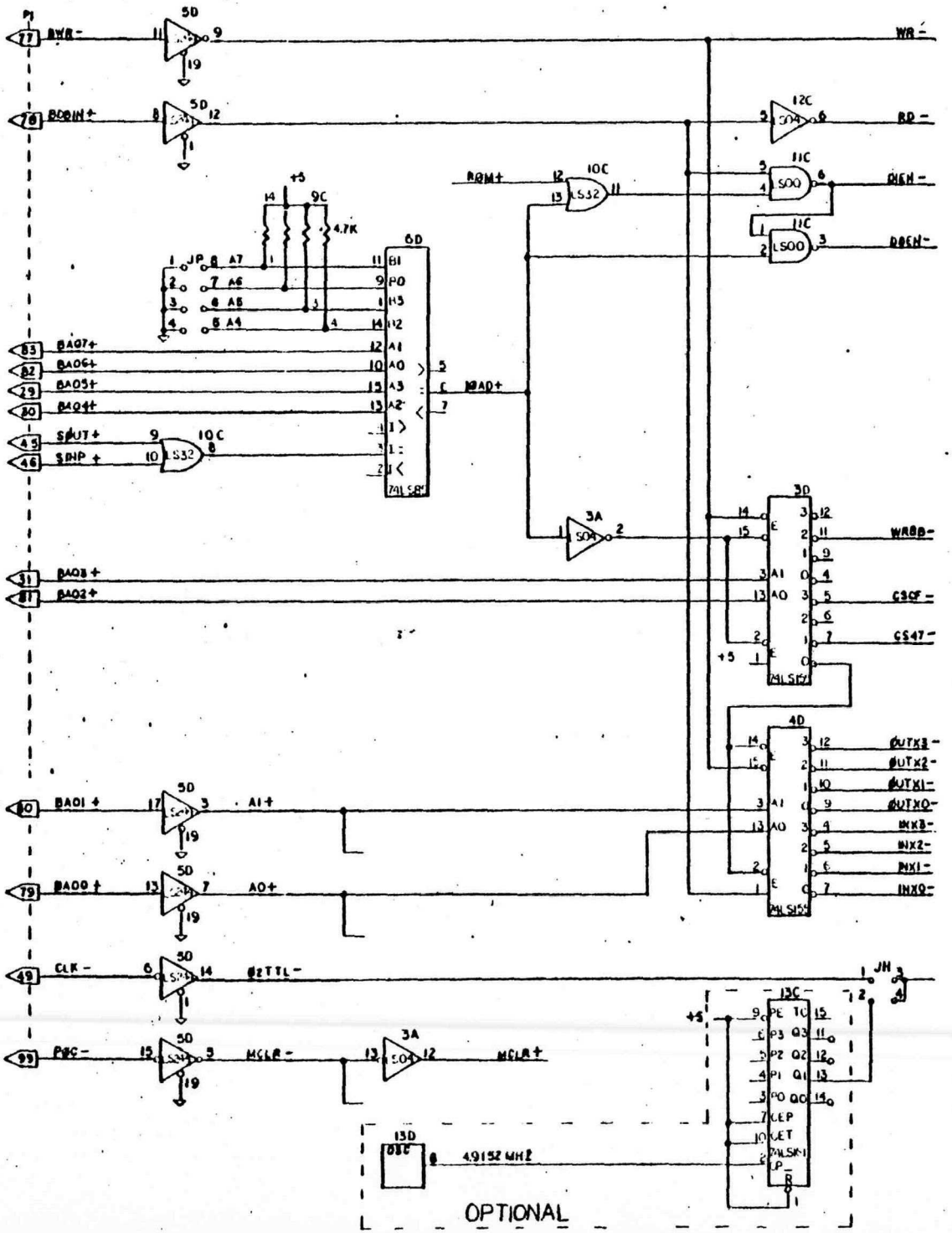
   JC 31-32

   PC4 JC 9-10 IP

   JC 23-24

   PC6 JC 13-20 ACK

   JC 14-19



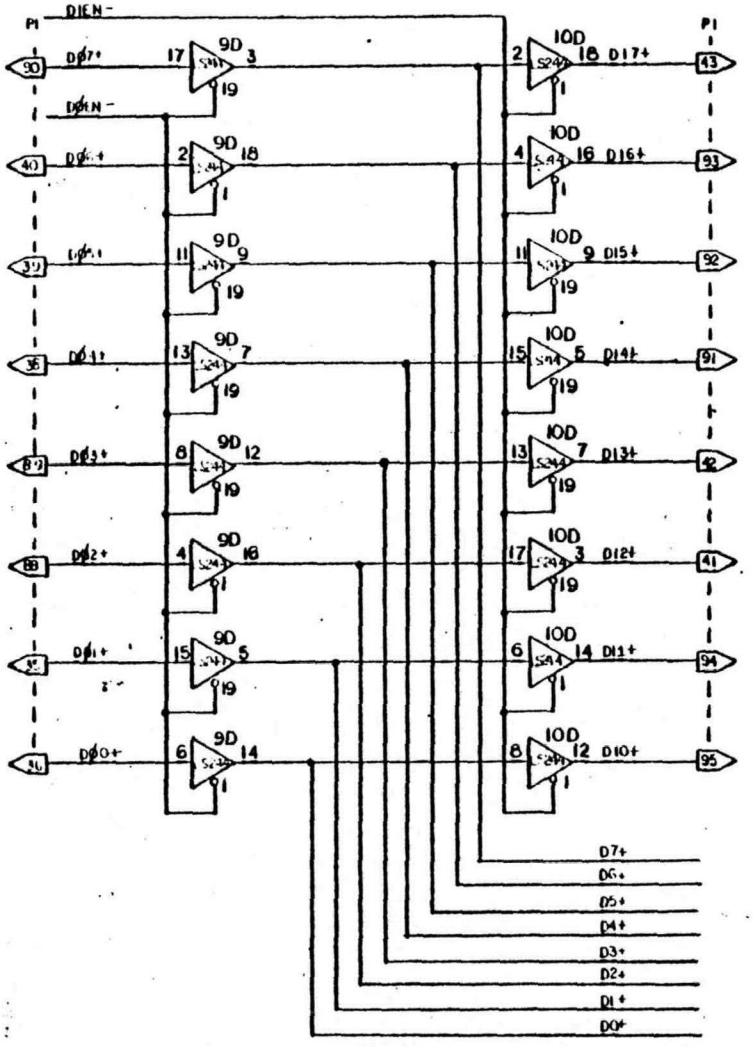
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

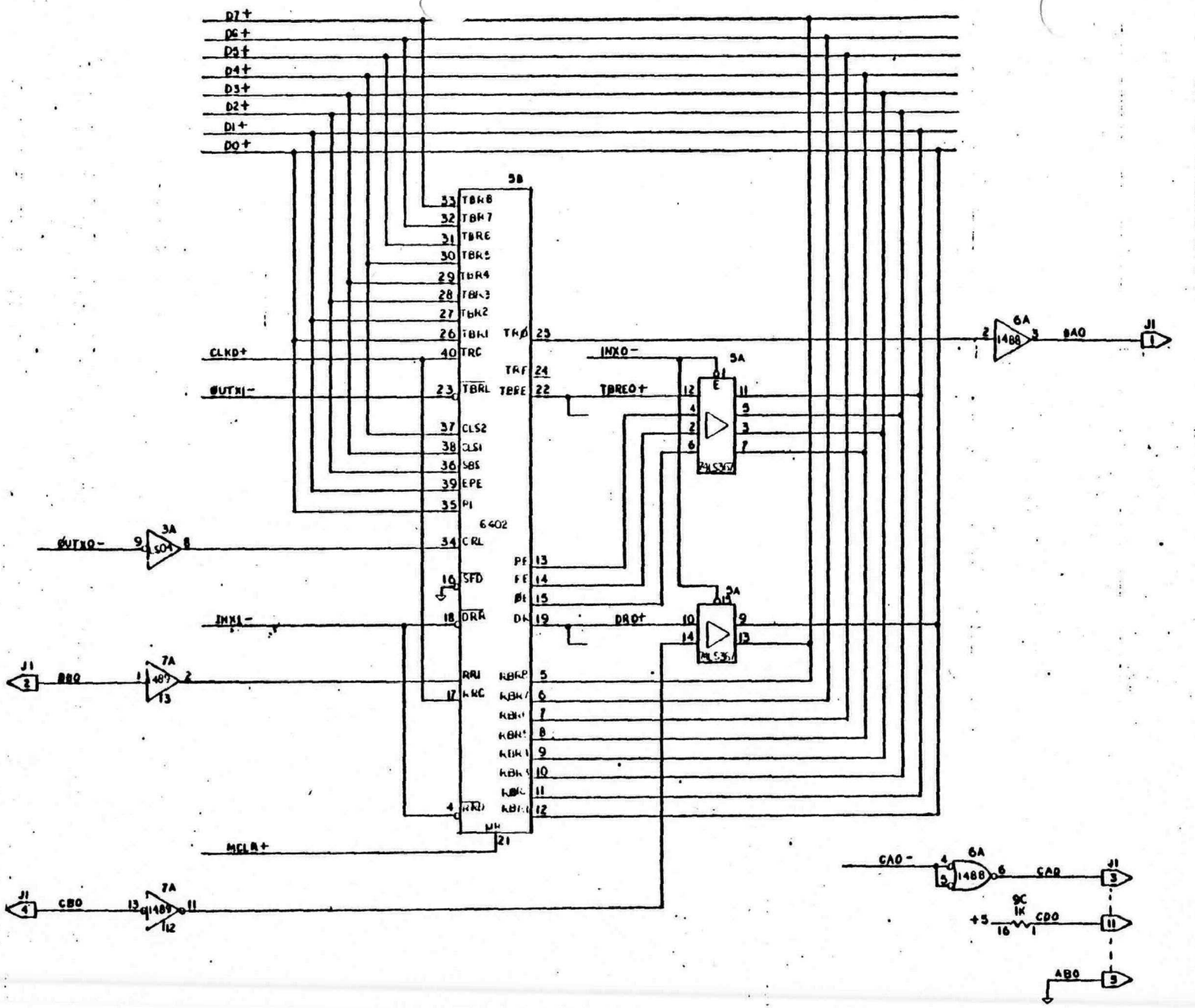
I/O BOARD

L00442

DRAWING NUMBER 1 OF 9



INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 2 OF 9



6402
VCC 1
GND 3

1488
VCC -14 - +12
VEE - 1 - -12
GND - 7

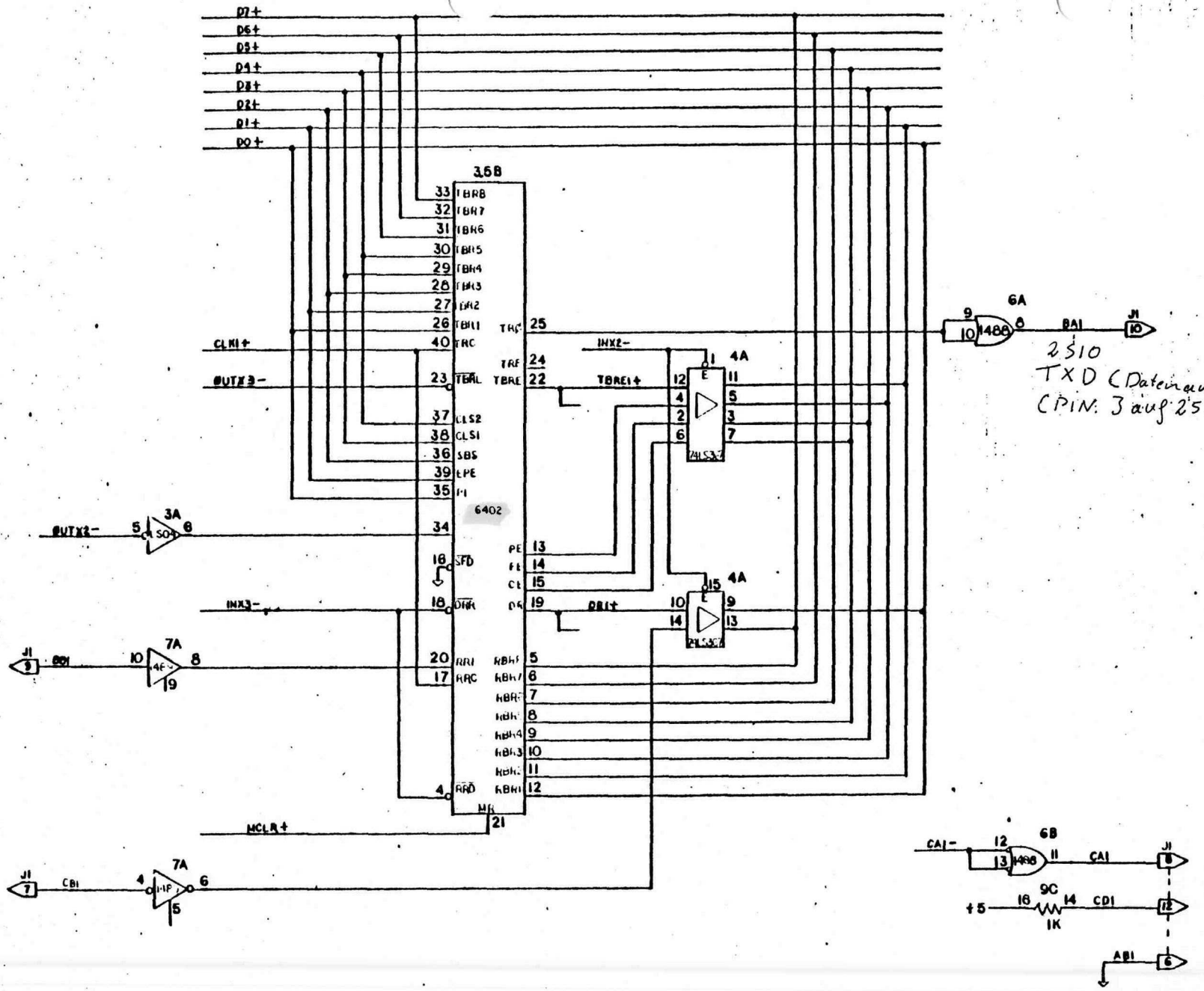
INDUSTRIAL MICRO SYSTEMS

SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED

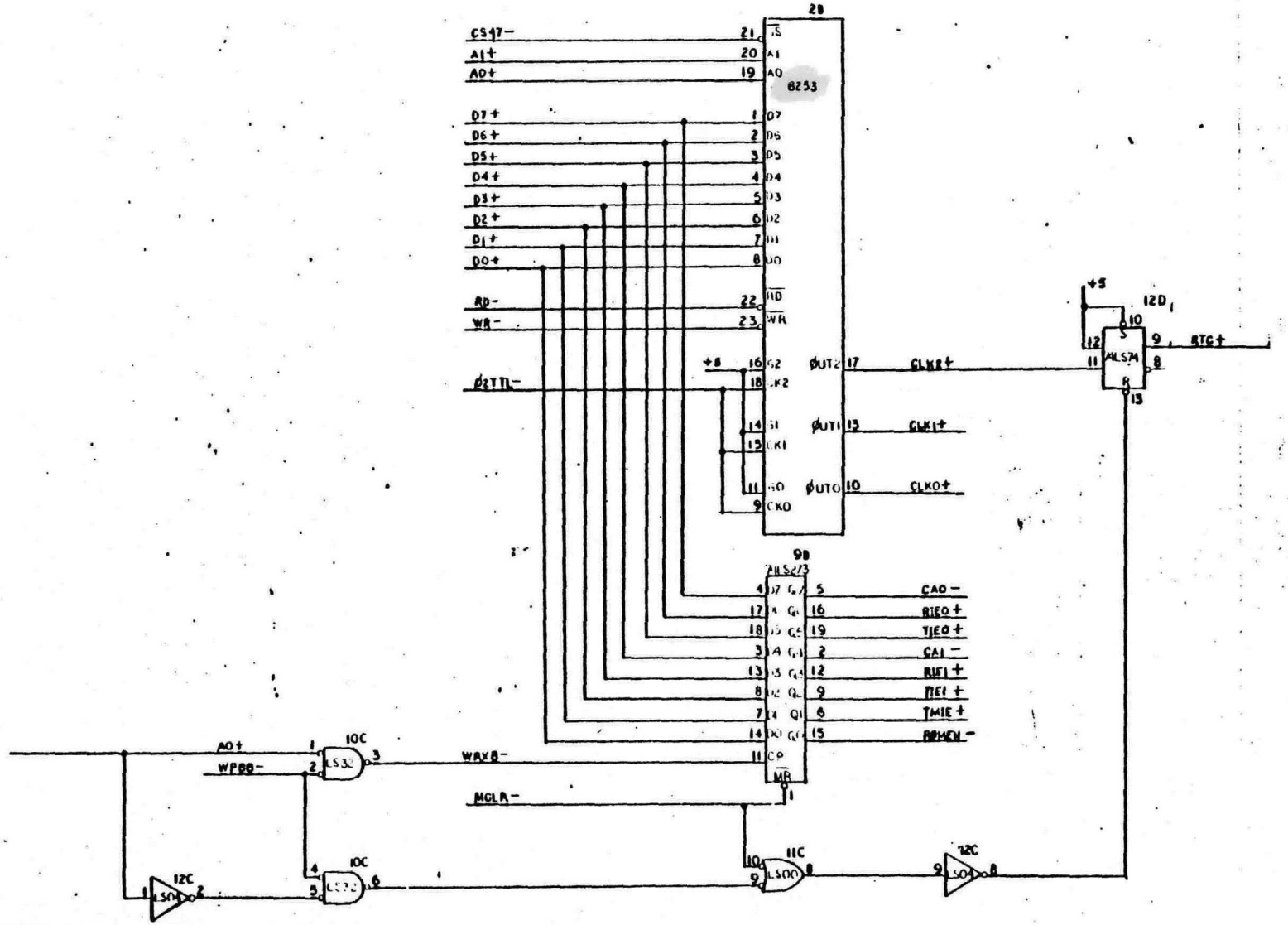
I/O BOARD

L00442

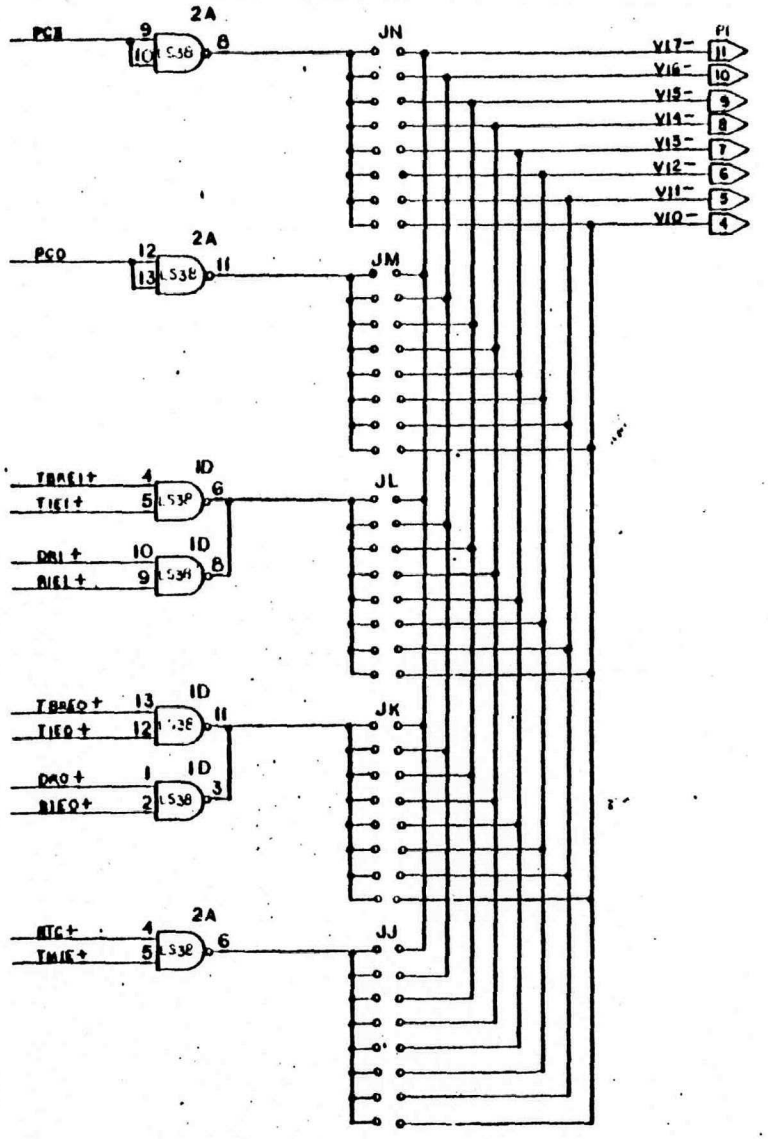
DRAWING NUMBER 3 OF 9

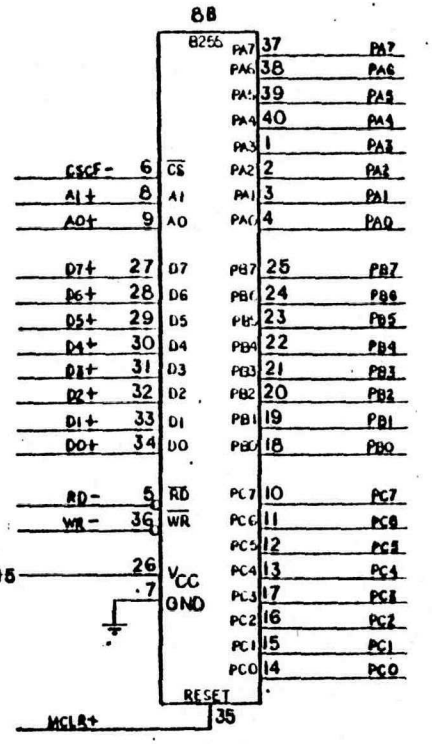


INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		4 OF 9

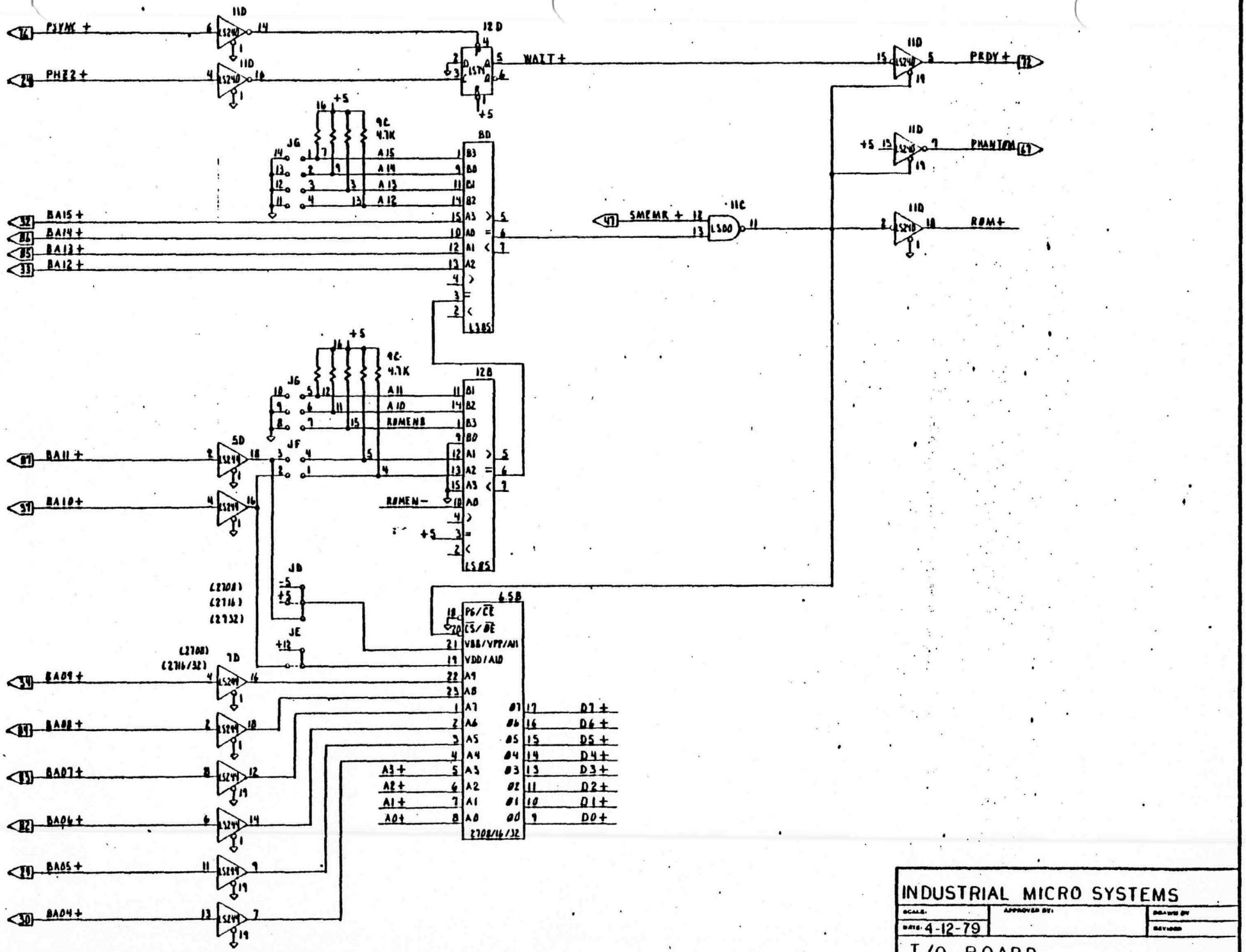


INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 5 OF 9

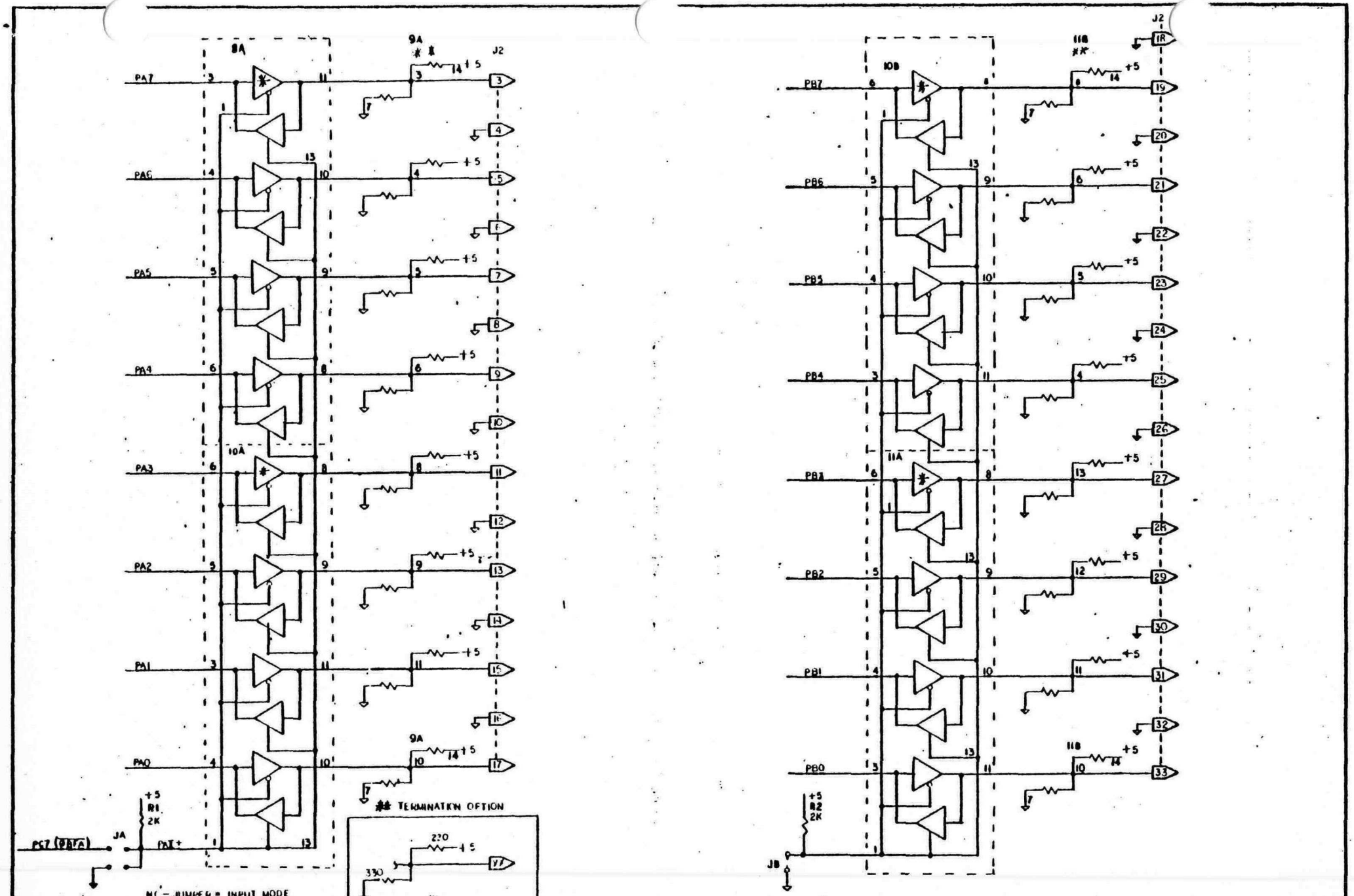




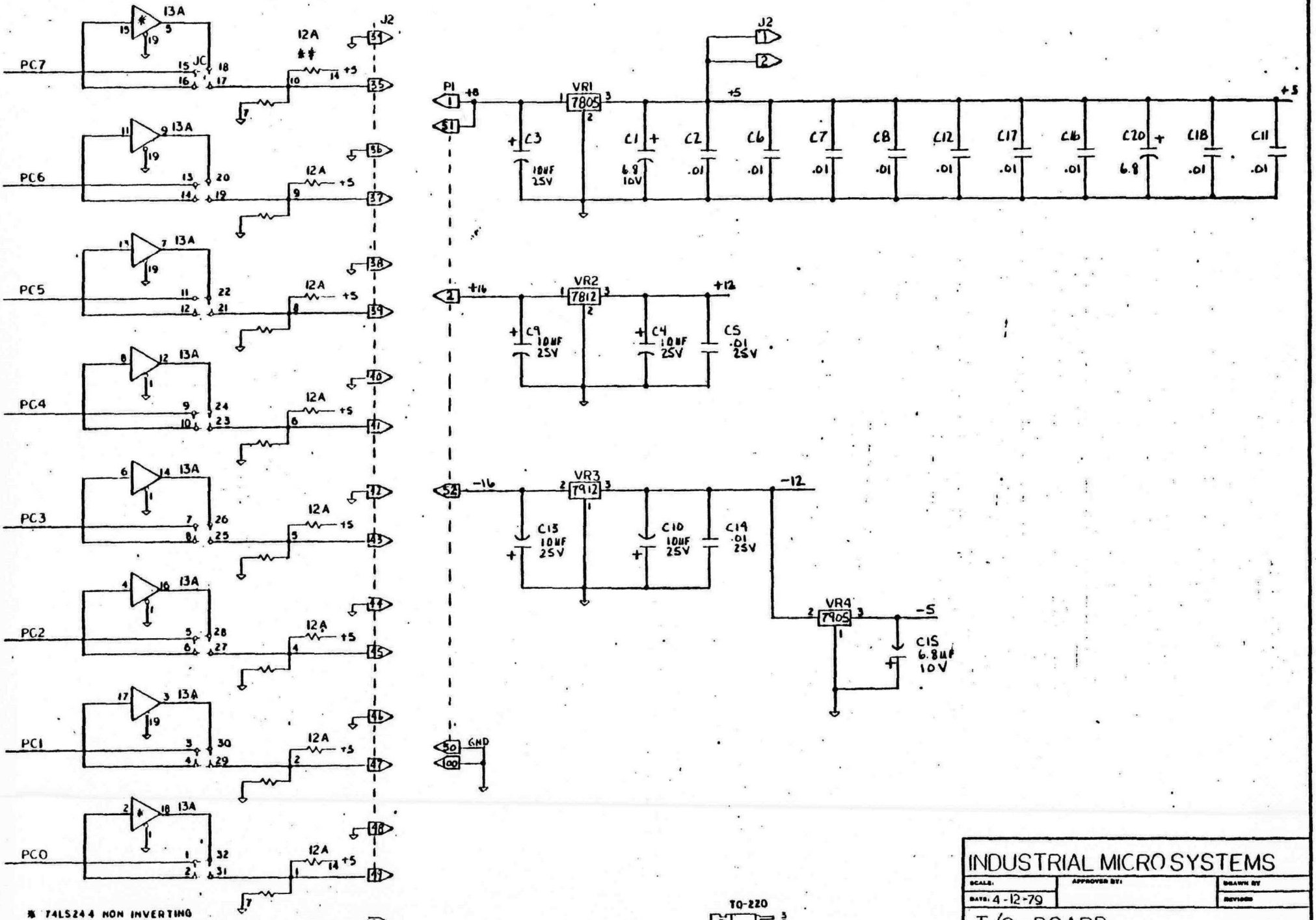
INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		DEVISED
I/O BOARD		
L00442		DRAWING NUMBER 6 OF 9

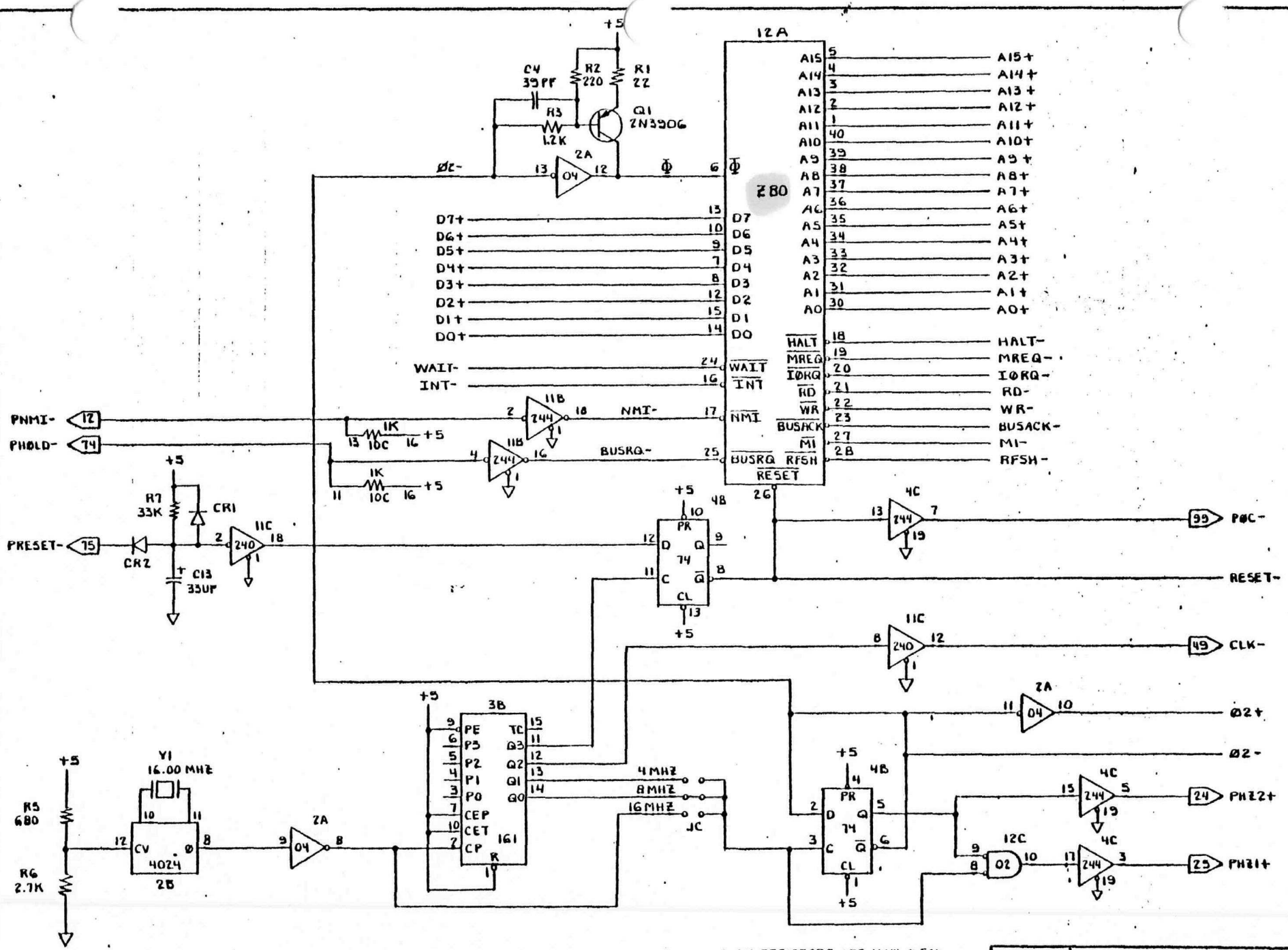


INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 7 OF 9



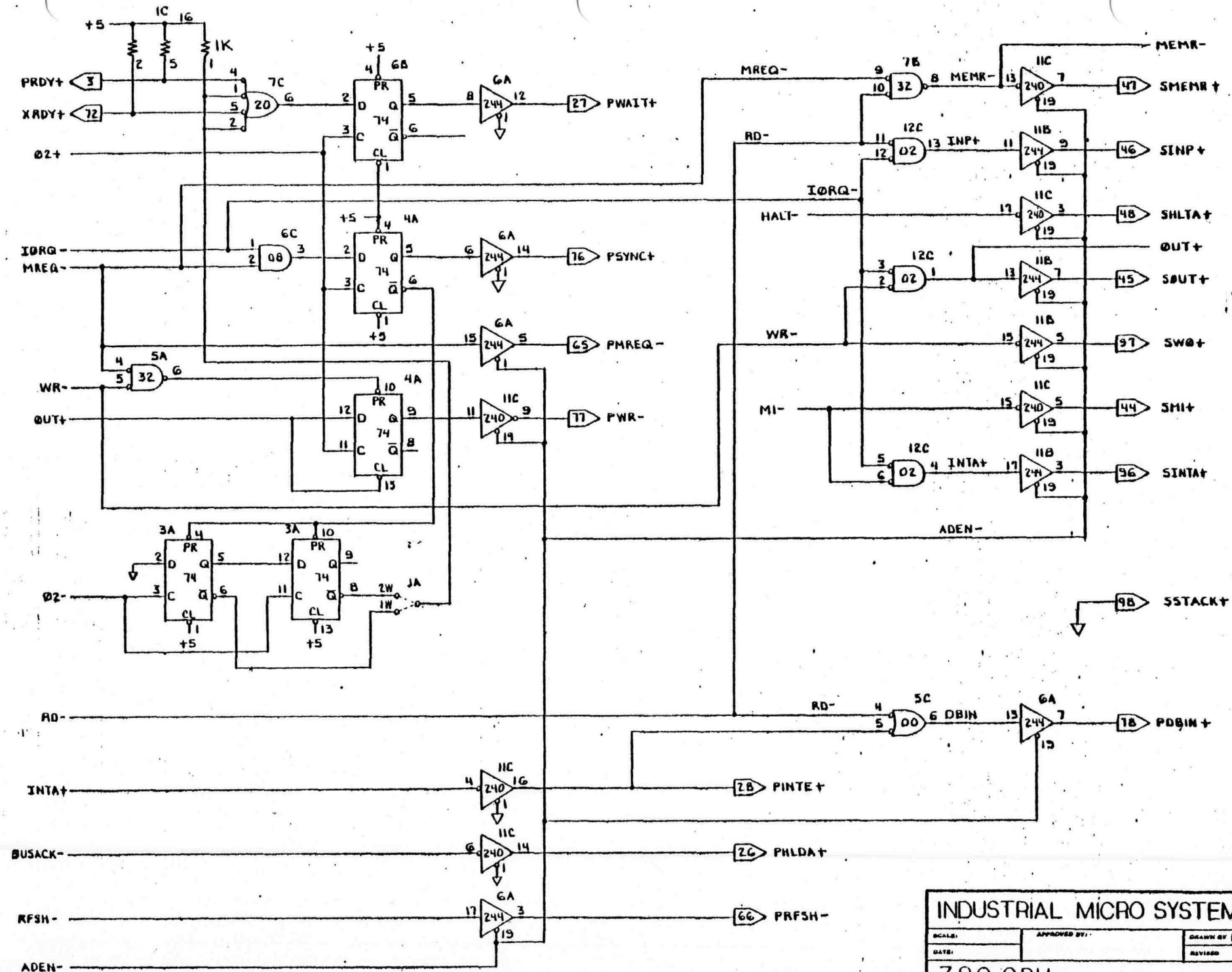
INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 4-12-79		REVISED
I/O BOARD		
L00442		DRAWING NUMBER 8 OF 9


PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
13A
12A
J2
JC
P1
VR1
7805
VR2
7812
VR3
7912
VR4
7905
+8
+16
-16
-12
-5
+5
+12
GND
C3 10UF 25V
C1 6.8 10V
C2 .01
C6 .01
C7 .01
C8 .01
C12 .01
C17 .01
C16 .01
C20 6.8
C18 .01
C11 .01
C9 10UF 25V
C4 10UF 25V
C5 .01 25V
C13 10UF 25V
C10 10UF 25V
C19 .01 25V
C15 6.8UF 10V
TO-220
* 74LS244 NON INVERTING
74LS240 INVERTING
INDUSTRIAL MICRO SYSTEMS
SCALE:
APPROVED BY:
DRAWN BY
DATE: 4-12-79
REVISED
I/O BOARD
L00442
DRAWING NUMBER
9 OF 9

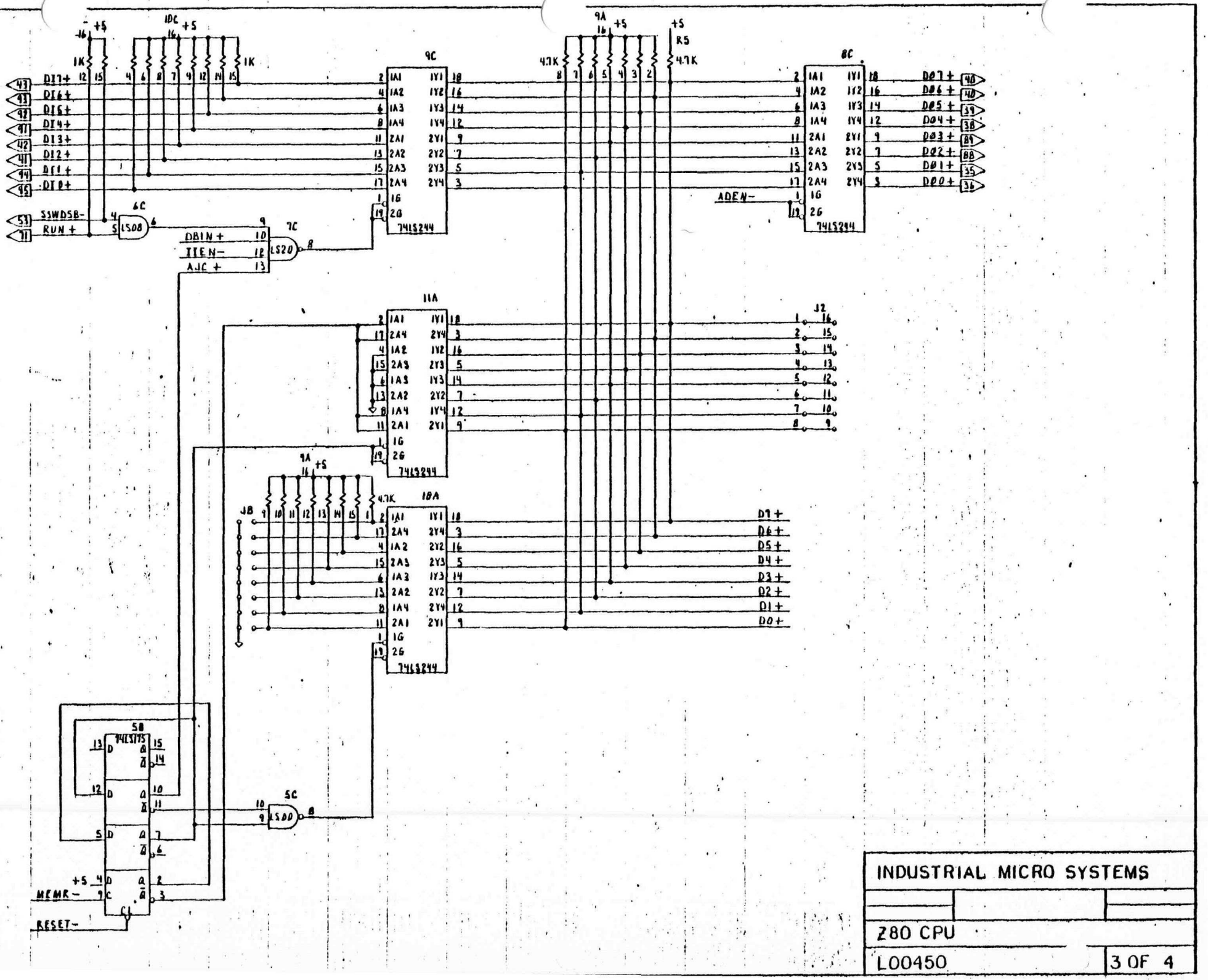


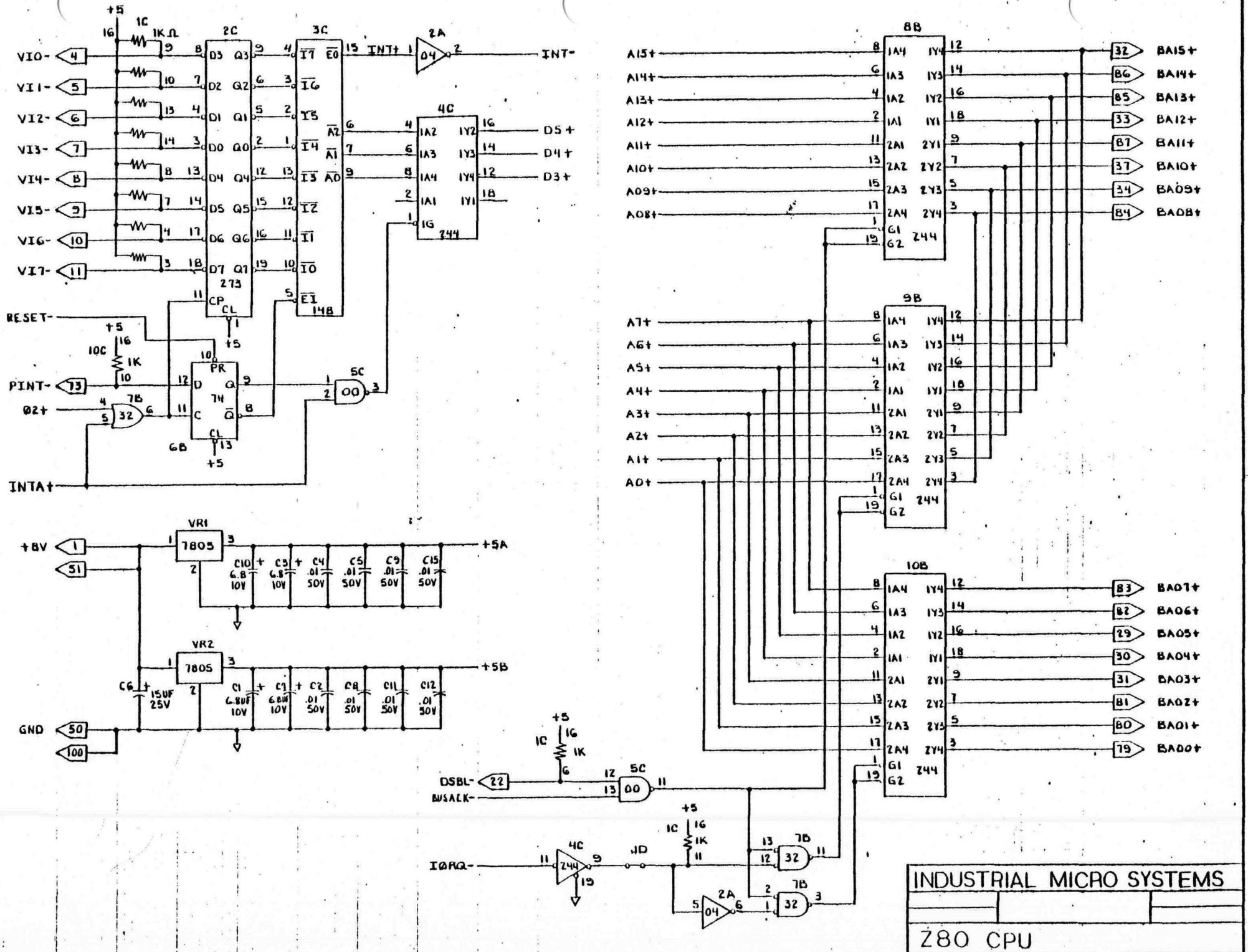
1. ALL RESISTORS ARE 1/4W ± 5%
2. ALL DIODES ARE SILICON SWITCHING

INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY RJV
DATE:		REVISED
Z80 CPU		
L00450.		DRAWING NUMBER SHT 1 OF 4



INDUSTRIAL MICRO SYSTEMS		
SCALE:	APPROVED BY:	DRAWN BY R.J.V
DATE:		REVISED
Z80 CPU		
L00450		DRAWING NUMBER 2 OF 4


INDUSTRIAL MICRO SYSTEMS
Z80 CPU
L00450
3 OF 4


INDUSTRIAL MICRO SYSTEMS
Z80 CPU
L00450
4 OF 4