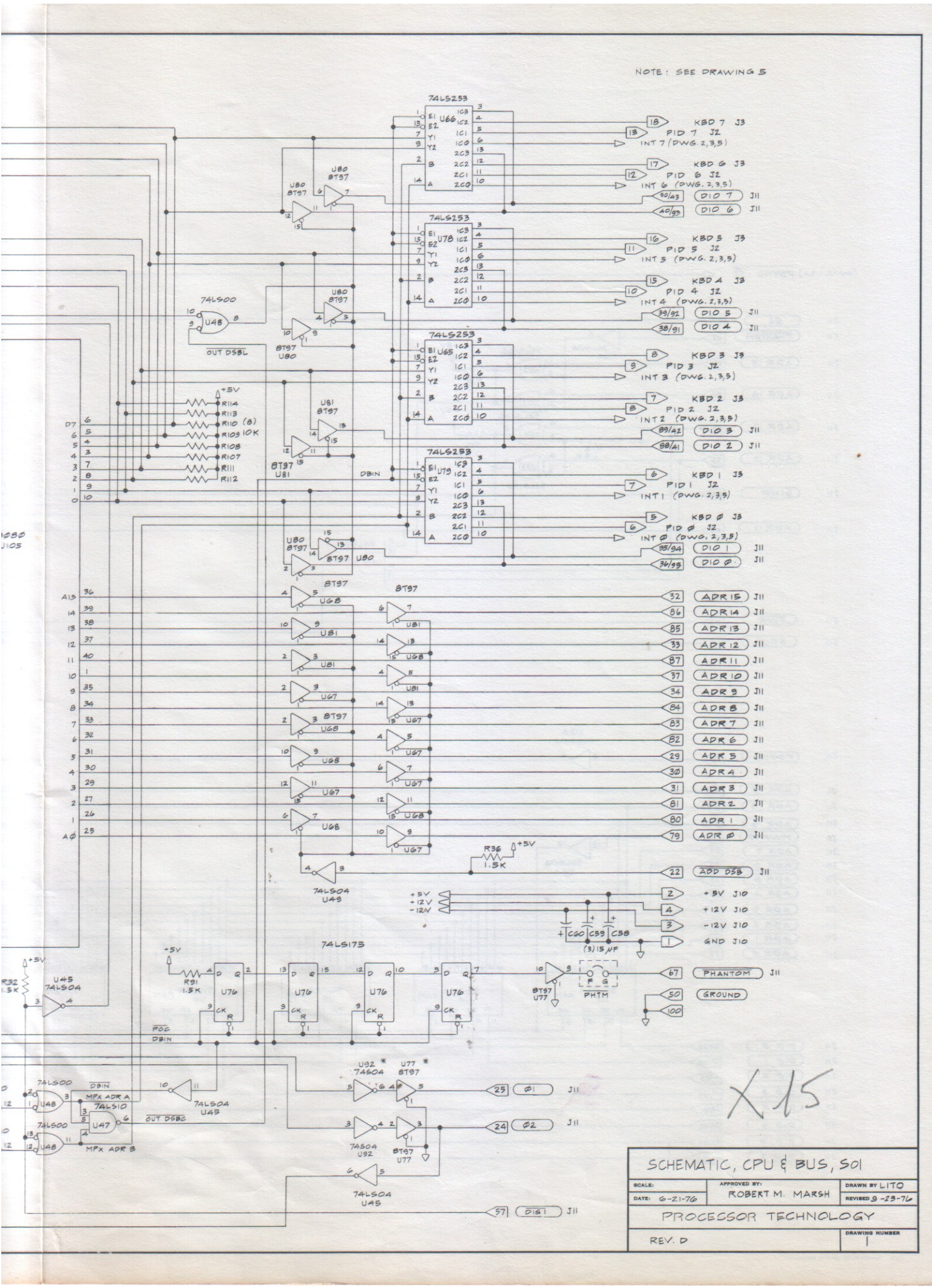
NOTE: SEE DRAWING 5
74LS253
U66
U78
U65
U79
74LS00
U48
U80 BT97
U81 BT97
U68
U67
74LS04
U45
74LS175
U76
74LS10
U47
R91 1.5K
R36 1.5K
R114
R113
R110 (8) 10K
R109
R108
R107
R111
R112
+5V
OUT DSBL
DBIN
MPX ADR A
MPX ADR B
OUT DSBC
POC
PHTM
BT97 U77
U82 74S04
KBD 7 J3
PID 7 J2
INT 7 (DWG. 2,3,5)
KBD 6 J3
PID 6 J2
INT 6 (DWG. 2,3,5)
KBD 5 J3
PID 5 J2
INT 5 (DWG. 2,3,5)
KBD 4 J3
PID 4 J2
INT 4 (DWG. 2,3,5)
KBD 3 J3
PID 3 J2
INT 3 (DWG. 2,3,5)
KBD 2 J3
PID 2 J2
INT 2 (DWG. 2,3,5)
KBD 1 J3
PID 1 J2
INT 1 (DWG. 2,3,5)
KBD Ø J3
PID Ø J2
INT Ø (DWG. 2,3,5)
DIO 7 J11
DIO 6 J11
DIO 5 J11
DIO 4 J11
DIO 3 J11
DIO 2 J11
DIO 1 J11
DIO Ø J11
ADR 15 J11
ADR 14 J11
ADR 13 J11
ADR 12 J11
ADR 11 J11
ADR 10 J11
ADR 9 J11
ADR 8 J11
ADR 7 J11
ADR 6 J11
ADR 5 J11
ADR 4 J11
ADR 3 J11
ADR 2 J11
ADR 1 J11
ADR Ø J11
ADD DSB J11
+5V J10
+12V J10
-12V J10
GND J10
C60 C59 C58
(3) 15 MF
PHANTOM J11
GROUND
Ø1 J11
Ø2 J11
DIS 1 J11
X 15
SCHEMATIC, CPU & BUS, SOL
SCALE:
DATE: 6-21-76
APPROVED BY: ROBERT M. MARSH
DRAWN BY LITO
REVISED 9-23-76
PROCESSOR TECHNOLOGY
REV. D
DRAWING NUMBER 1