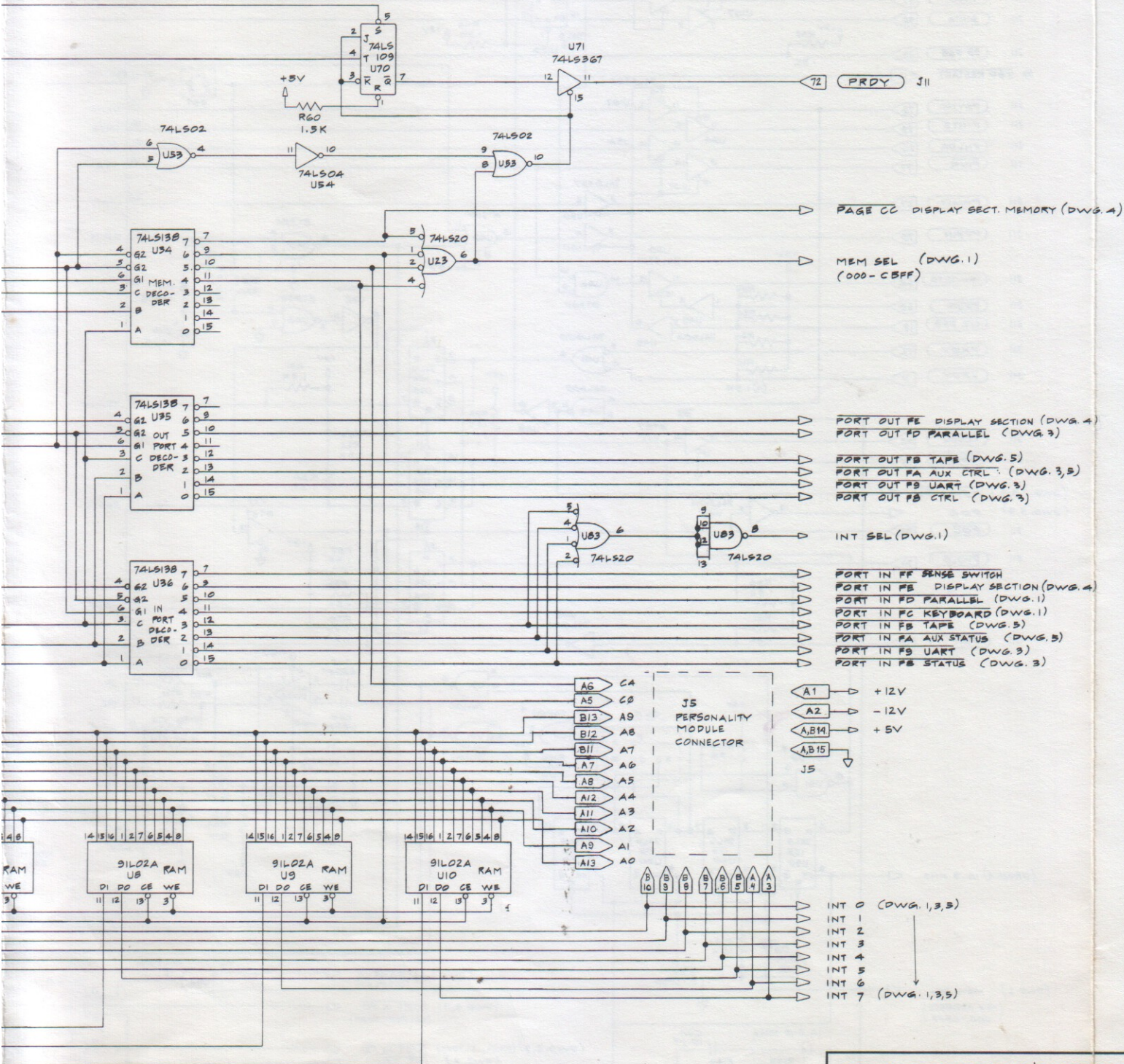


X16

NOTE: SEE DRAWING 5



SCHEMATIC, MEMORY & DECODER, Sol

SCALE:	APPROVED BY:	DRAWN BY LITC
DATE: 6/15/76	ROBERT M. MARSH	REVISED 9-23-
PROCESSOR TECHNOLOGY		
REV. D	DRAWING NUMBER 2	