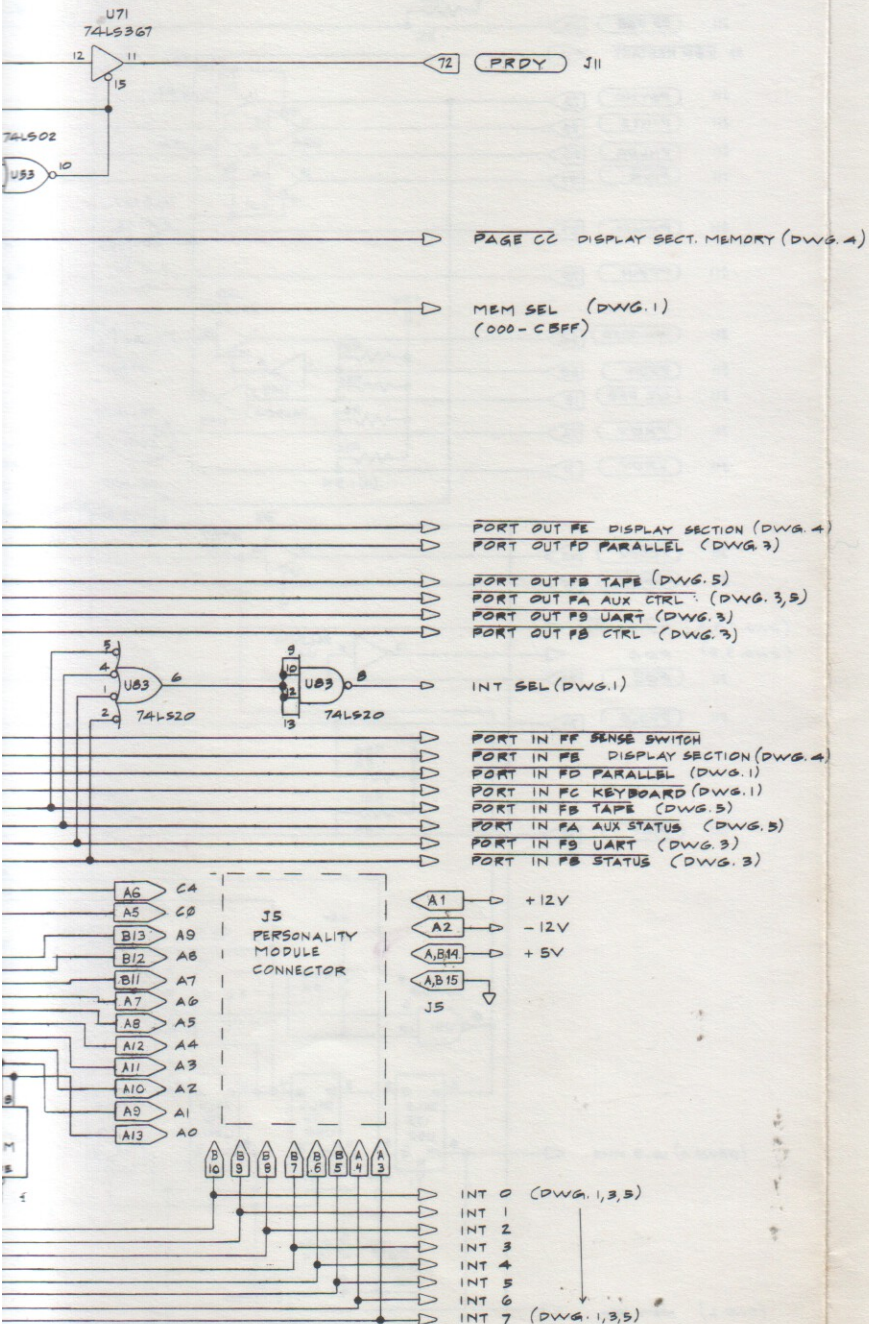


X16

NOTE: SEE DRAWING 5



SCHEMATIC, MEMORY & DECODER, SOI

SCALE:	APPROVED BY:	DRAWN BY L10
DATE: 6/15/76	ROBERT M. MARSH	REVISED 9-23-76
PROCESSOR TECHNOLOGY		
REV. D	DRAWING NUMBER 2	