

S-100 Bus Definitions-continued

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---------------|--------|---------------------|--|
| 27 | PWAIT | WAIT | -Processor command/control signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle |
| 28 | PINTE | INTERRUPT ENABLE | -Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited. |
| 29 | A5 | Address Line #5 | |
| 30 | A4 | Address Line #4 | |
| 31 | A3 | Address Line #3 | |
| 32 | A15 | Address Line #15 | (MSB) |
| 33 | A12 | Address Line #12 | |
| 34 | A9 | Address Line #9 | |
| 35 | DIO1 | Data In/Out line #1 | same as pin 94 |
| 36 | DIO0 | Data In/Out line #0 | same as pin 95 |
| 37 | A10 | Address Line #10 | |
| 38 | DIO4 | Data In/Out Line #4 | same as pin 91 |
| 39 | DIO5 | Data In/Out Line #5 | same as pin 92 |
| 40 | DIO6 | Data In/Out Line #6 | same as pin 93 |
| 41 | DIO2 | Data In/Out Line #2 | same as pin 88 |
| 42 | DIO3 | Data In/Out Line #3 | same as pin 89 |
| 43 | DIO7 | Data In/Out Line #7 | same as pin 90 |
| 44 | SM1 | MACHINE CYCLE 1 | -Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction |
| 45 | SOUT | OUTPUT | -Status output signal that indicates the address bus contains the address of an output device and the data bus will contain the output data when PWR is active |
| 46 | SINP | INPUT | -Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active |
| 47 | SMEMR | MEMORY READ | -Status output signal that indicates the data bus will be used to read memory data |
| 48 | SHLTA | HALT ACKNOWLEDGE | -Status output signal that acknowledges a HALT instruction |
| 49 | CLOCK | CLOCK | - Inverted output of the 02 CLOCK |
| 50 | GND | GROUND | |
| 51 | +8V | +8 Volts | Unregulated input to 5 volt regulators supplied by Sol-20 power supply |
| 52 | -16V | -16 Volts | Negative unregulated voltage supplied by Sol-20 power supply |