S-100 Bus Definitions-continued

PIN NUMBER	SYMBOL	NAME	FUNCTION
53	SSWI EXT CLR	SENSE SWITCH INPUT EXTERNAL CLEAR	not used by Sol-PC electronics
54 55	RTC	REAL TIME CLOCK	not used by Sol-PC electronics
56	STSTB	STATUS STROBE DATA INPUT GATE #1	not used by Sol When low forces PDBINS low and
57	DIG1	DATA INFUL GALE #1	forces CPU input multiplexers to the DIO bus. During CPU DBIN cycle, disables CPU DIO bus drivers
58 59	FRDY	FRONT PANEL READY	-When low disables MWRITE driver
to	TO BE DEFINED		
64	MREQ	MEMORY REQUEST	-Z 80 signal not used by Sol-PC electronics
66	REF	REFRESH	- Z 80 signal not used by Sol-PC electronics
67	PHANTOM	PHANTOM DISABLE	-Output from CPU section used to disable RAM or ROM during power on initialization program execution
68	MWRITE	MEMORY WRITE	-Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus
69	PS	PROJECT STATUS	-not used by Sol-PC electronics
70	PROT	PROTECT	-not used by Sol-PC electronics -not used by Sol-PC electronics
71 72	RUN PRDY	RUN PROCESSOR READY	- Memory and I/O input to the CPU Board wait circuitry
73	PINT	INTERRUPT REQUEST	- The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request. -Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current
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		RESET	<pre>machine cycle -Processor command/control input;</pre>
			while activated, the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	-Processor command/control output; provides a signal to indicate the
	PWR	WRITE Designation ?	beginning of each machine cycle -Processor command/control output; used for memory write or I/O out-
		Unregulators auppl	put control. Data on the data <u>bus</u> is stable while the PWR is active
78	PDBIN	DATA BUS IN	-Processor command/control output; indicates to external circuits that the data bus is in the input mode
			the data bus is in the input mode