APPENDICES

Processor Technology

Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit directly from **Processor Technology** and returned to the factory within the three-month warranty period, which in the judgement of **PTC** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, without charge. Kits purchased from authorized **PTC** dealers should be returned to the selling dealer for the same warranty service.

Any modules purchased as a kit and returned to **PTC,** which in the judgement of **PTC** are not covered by the above conditions, will be repaired and returned at a cost commensurate with the work required. In any case, this charge will not exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

Hex	Instruction	Hex	Instruction	Hex	Instruction	Hex	Instruction	Hex	Instruction	Hex	Instruction	Hex	Instruction
00	NOP	28	---	50	MOV D,B	78	MOV A,B	A0	ANA B	C8	RZ	F0	RP
01	LXI B,D16	29	DAD H	51	MOV D,C	79	MOV A,C	A1	ANA C	C9	RET	F1	POP PSW
02	STAX B	2A	LHLD Adr	52	MOV D,D	7A	MOV A,D	A2	ANA D	CA	JZ	F2	JP Adr
03	INX B	2B	DCX H	53	MOV D,E	7B	MOV A,E	A3	ANA E	CB	---	F3	DI
04	INR B	2C	INR L	54	MOV D,H	7C	MOV A,H	A4	ANA H	CC	CZ Adr	F4	CP Adr
05	DCR B	2D	DCR L	55	MOV D,L	7D	MOV A,L	A5	ANA L	CD	CALL Adr	F5	PUSH PSW
06	MVI B,D8	2E	MVI L,D8	56	MOV D,M	7E	MOV A,M	A6	ANA M	CE	ACI D8	F6	ORI D8
07	RLC	2F	CMA	57	MOV D,A	7F	MOV A,A	A7	ANA A	CF	RST 1	F7	RST 6
08	---	30	---	58	MOV E,B	80	ADD B	A8	XRA B	D0	RNC	F8	RM
09	DAD B	31	LXI SP,D16	59	MOV E,C	81	ADD C	A9	XRA C	D1	POP D	F9	SPHL
0A	LDAX B	32	STA Adr	5A	MOV E,D	82	ADD D	AA	XRA D	D2	JNC Adr	FA	JM Adr
0B	DCX B	33	INX SP	5B	MOV E,E	83	ADD E	AB	XRA E	D3	OUT D8	FB	EI
0C	INR C	34	INR M	5C	MOV E,H	84	ADD H	AC	XRA H	D4	CNC Adr	FC	CM Adr
0D	DCR C	35	DCR M	5D	MOV E,L	85	ADD L	AD	XRA L	D5	PUSH D	FD	---
0E	MVI C,D8	36	MVI M,D8	5E	MOV E,M	86	ADD M	AE	XRA M	D6	SUI D8	FE	CPI D8
0F	RRC	37	STC	5F	MOV E,A	87	ADD A	AF	XRA A	D7	RST 2	FF	RST 7
10	---	38	---	60	MOV H,B	88	ADC B	B0	ORA B	D8	RC		
11	LXI D,D16	39	DAD SP	61	MOV H,C	89	ADC C	B1	ORA C	D9	---		
12	STAX D	3A	LDA Adr	62	MOV H,D	8A	ADC D	B2	ORA D	DA	JC Adr		
13	INX D	3B	DCX SP	63	MOV H,E	8B	ADC E	B3	ORA E	DB	IN D8		
14	INR D	3C	INR A	64	MOV H,H	8C	ADC H	B4	ORA H	DC	CC Adr		
15	DCR D	3D	DCR A	65	MOV H,L	8D	ADC L	B5	ORA L	DD	---		
16	MVI D,D8	3E	MVI A,D8	66	MOV H,M	8E	ADC M	B6	ORA M	DE	SBI D8		
17	RAL	3F	CMC	67	MOV H,A	8F	ADC A	B7	ORA A	DF	RST 3		
18	---	40	MOV B,B	68	MOV L,B	90	SUB B	B8	CMP B	E0	RPO		
19	DAD D	41	MOV B,C	69	MOV L,C	91	SUB C	B9	CMP C	E1	POP H		
1A	LDAX D	42	MOV B,D	6A	MOV L,D	92	SUB D	BA	CMP D	E2	JPO Adr		
1B	DCX D	43	MOV B,E	6B	MOV L,E	93	SUB E	BB	CMP E	E3	XTHL		
1C	INR E	44	MOV B,H	6C	MOV L,H	94	SUB H	BC	CMP H	E4	CPO Adr		
1D	DCR E	45	MOV B,L	6D	MOV L,L	95	SUB L	BD	CMP L	E5	PUSH H		
1E	MVI E,D8	46	MOV B,M	6E	MOV L,M	96	SUB M	BE	CMP M	E6	ANI D8		
1F	RAR	47	MOV B,A	6F	MOV L,A	97	SUB A	BF	CMP A	E7	RST 4		
20	---	48	MOV C,B	70	MOV M,B	98	SBB B	C0	RNZ	E8	RPE		
21	LXI H,D16	49	MOV C,C	71	MOV M,C	99	SBB C	C1	POP B	E9	PCHL		
22	SHLD Adr	4A	MOV C,D	72	MOV M,D	9A	SBB D	C2	JNZ Adr	EA	JPE Adr		
23	INX H	4B	MOV C,E	73	MOV M,E	9B	SBB E	C3	JMP Adr	EB	XCHG		
24	INR H	4C	MOV C,H	74	MOV M,H	9C	SBB H	C4	CNZ Adr	EC	CPE Adr		
25	DCR H	4D	MOV C,L	75	MOV M,L	9D	SBB L	C5	PUSH B	ED	---		
26	MVI H,D8	4E	MOV C,M	76	HLT	9E	SBB M	C6	ADI D8	EE	XRI D8		
27	DAA	4F	MOV C,A	77	MOV M,A	9F	SBB A	C7	RST 0	EF	RST 5		

HEX-ASCII TABLE

Printing		Characters	
30	0	40	@
31	1	20	space
32	2	21	!
33	3	22	"
34	4	23	#
35	5	24	$
36	6	25	%
37	7	26	&
38	8	27	'
39	9	28	(
		29	)
41	A	2A	*
42	B	2B	+
43	C	2C	,
44	D	2D	−
45	E	2E	.
46	F	2F	/
47	G	3A	:
48	H	3B	;
49	I	3C	<
4A	J	3D	=
4B	K	3E	>
4C	L	3F	?
4D	M	5B	[
4E	N	5C	\
4F	O	5D	]
50	P	5E	↑ (∧)
51	Q	5F	← (−)
52	R		
53	S		
54	T		
55	U		
56	V		
57	W		
58	X		
59	Y		
5A	Z		

HEX-ASCII TABLE

Non-Printing	
00	NULL
07	BELL
09	TAB
0A	LF
0B	VT
0C	FORM
0D	CR
11	X-ON
12	TAPE
13	X-OFF
14	
1B	ESC
7D	ALT MODE
7F	RUB OUT

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

Processor Technology Corp.

APPENDIX II

JUMP

C3	JMP	Adr
C2	JNZ	Adr
CA	JZ	Adr
D2	JNC	Adr
DA	JC	Adr
E2	JPO	Adr
EA	JPE	Adr
F2	JP	Adr
FA	JM	Adr
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	Adr
CC	CZ	Adr
D4	CNC	Adr
DC	CC	Adr
E4	CPO	Adr
EC	CPE	Adr
F4	CP	Adr
FC	CM	Adr

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE IMMEDIATE

06	MVI	B,	D8
0E	MVI	C,	D8
16	MVI	D,	D8
1E	MVI	E,	D8
26	MVI	H,	D8
2E	MVI	L,	D8
36	MVI	M,	D8
3E	MVI	A,	D8

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	D8
D6	SUI	D8
DE	SBI	D8
E6	ANI	D8
EE	XRI	D8
F6	ORI	D8
FE	CPI	D8

LOAD IMMEDIATE

01	LXI	B,	D16
11	LXI	D,	D16
21	LXI	H,	D16
31	LXI	SP	D16

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

SPECIALS

EB	XCHG
27	DAA*
2F	CMA
37	STC†
3F	CMC†

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MCV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

ACCUMULATOR*

80	ADD	B	A8	XRA	B
81	ADD	C	A9	XRA	C
82	ADD	D	AA	XRA	D
83	ADD	E	AB	XRA	E
84	ADD	H	AC	XRA	H
85	ADD	L	AD	XRA	L
86	ADD	M	AE	XRA	M
87	ADD	A	AF	XRA	A
88	ADC	B	B0	ORA	B
89	ADC	C	B1	ORA	C
8A	ADC	D	B2	ORA	D
8B	ADC	E	B3	ORA	E
8C	ADC	H	B4	ORA	H
8D	ADC	L	B5	ORA	L
8E	ADC	M	B6	ORA	M
8F	ADC	A	B7	ORA	A
90	SUB	B	B8	CMP	B
91	SUB	C	B9	CMP	C
92	SUB	D	BA	CMP	D
93	SUB	E	BB	CMP	E
94	SUB	H	BC	CMP	H
95	SUB	L	BD	CMP	L
96	SUB	M	BE	CMP	M
97	SUB	A	BF	CMP	A
98	SBB	B			
99	SBB	C			
9A	SBB	D			
9B	SBB	E			
9C	SBB	H			
9D	SBB	L			
9E	SBB	M			
9F	SBB	A			
A0	ANA	B			
A1	ANA	C			
A2	ANA	D			
A3	ANA	E			
A4	ANA	H			
A5	ANA	L			
A6	ANA	M			
A7	ANA	A			

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[ ]
DW	D16	[ ]

CONSTANT DEFINITION

0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A' 'B'	ASCII

OPERATORS

\+ –

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

* = all Flags (C,Z,S,P) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

APPENDIX II

STANDARD COLOR CODE FOR RESISTORS AND CAPACITORS

COLOR	SIGNIFICANT FIGURE	DECIMAL MULTIPLIER	TOLERANCE (%)	VOLTAGE RATING*
Black	0	1		--
Brown	1	10		100
Red	2	100		200
Orange	3	1,000		300
Yellow	4	10,000		400
Green	5	100,000		500
Blue	6	1,000,000		600
Violet	7	10,000,000		700
Gray	8	100,000,000		800
White	9	1,000,000,000		900
Gold	-	0.1	5	1000
Silver	-	0.01	10	2000
No Color	-	---	20	500

*Applies to capacitors only.

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alighment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45° angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron--25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder

melts the rest of the joint will be hot enough for the solder to "take", (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

INSTALLING AUGAT PINS

Augat pins are normally supplied on carriers (e.g., 8-pin and 16-pin carriers). In many cases the PC board layout permits Augat pins to be installed while still attached to the carrier or a portion of the carrier. In other cases the pins must be installed singly.

To install two or more pins that are still attached to the carrier, proceed as follows:

NOTE

It is perfectly alright to appropriately cut a carrier to accommodate the installation. For example, an 8-pin carrier can be cut in half (4 pins each) across the short dimension to fit a 4-pin, 4-corner layout. It may also be cut in half along the long dimension to fit a 4-pin, inline layout.

(1) Insert pins in the mounting holes from the front (component) side of board. (The carrier will hold the pins perpendicular to the board.)

(2) Solder all pins from back (solder) side of board so the solder "wicks up" to the front side.

(3) Check for solder bridges.

(4) Remove carrier.

To install single pins, proceed as follows:

(1) Hold board between two objects so that it stands on edge.

(2) Insert pins in the mounting holes from front (component) side of board.

(3) Solder pins from back (solder) side of board so the solder "wicks up" to the front side. (This will hold the pins firmly in place.)

(4) Insert a component lead into one pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible. Remove component lead. Repeat this procedure with other pins.

<u>NOTE</u>

If cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

(5) Check each installation for cold joints and solder bridges.

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Television Interface

Anyone with a bunch of memory circuits, control logic and a wire wrap gun can whip up a digital video generator with TTL output levels. The problem as I see it is to get that digital video signal into a form that the TV set can digest. The care and feeding of digital inputs to the TV set is the subject of Don Lancaster's contribution to BYTE 2 – an excerpt from his forthcoming book, *TV Typewriter Cookbook*, to be published by Howard W. Sams, Indianapolis, Indiana.

. CARL

by
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We can get between a TV typewriter and a television style display system either by an rf modulator or a direct video method.

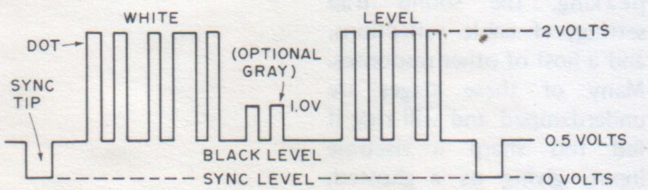
In the rf modulator method, we build a miniature, low power, direct wired TV transmitter that clips onto the antenna terminals of the TV set. This has the big advantage of letting you use any old TV set and ending up with an essentially free display that can be used just about anywhere. No set modifications are needed, and you have the additional advantage of automatic safety isolation and freedom from hot chassis shock problems.

There are two major restrictions to the rf modulator method. The first of these is that transmitters of this type must meet certain exactly spelled out FCC regulations and that system type approval is required. The second limitation is one of bandwidth. The best you can possibly hope for is 3.5 MHz for black and white and only 3 MHz for color, and many economy sets will provide far less. Thus, long character line lengths, sharp characters, and premium (lots of dots) character generators simply aren't compatible with clip-on rf entry.

In the direct video method, we enter the TV set immediately following its video detector but before sync is picked off. A few premium TV sets and all monitors already have a video input directly available, but these are still expensive and rare. Thus, you usually have to modify your TV set, either adding a video input and a selector switch or else dedicating the set to exclusive TV typewriter use. Direct video eliminates the bandwidth restrictions provided by the tuner, i-f strip, and video detector filter. Response can be further extended by removing or shorting the 4.5 MHz sound trap and by other modifications to provide us with longer line lengths and premium characters. No FCC approval is needed, and several sets or monitors are easily driven at once without complicated distribution problems.

There are two limitations to the direct video technique. One is that the set has to be modified to provide direct video entry. A second, and far more severe, restriction, is that many television sets are "hot chassis" or ac-dc sets with one side of their chassis connected to the power line. These sets introduce a severe shock hazard and cannot be used as TV typewriter video entry displays unless some isolation technique is used with them. If the TV set has a power transformer, there is usually no hot chassis problem. Transistor television sets and IC sets using no vacuum tubes tend to have power transformers, as do older premium tube type sets. All others (around half the sets around today) do not.

Fig. 1. Standard video interface levels. (Source impedance = 72 or 100 Ohms.)



Direct Video Methods

With either interface approach, we usually start by getting the dot matrix data, blanking, cursor, and sync signals together into one composite video signal whose form is useful to monitors and TV sets. A good set of standards is shown in Fig. 1. The signal is dc coupled and always positive going. Sync tips are grounded and blacker than black. The normal open circuit black level is positive by one-half a volt, and the white level is two volts positive. In most TV camera systems, intermediate levels between the half volt black level and the two volt white level will be some shade of gray, proportionately brighter with increasing positive voltage. With most TV typewriter systems, only the three states of zero volts (sync), half a volt (black), and two volts (white dot) would be used. One possible exception would be an additional one volt dot level for a dim but still visible portion of a message or a single word.

The usual video source impedance is either 72 or 100 Ohms. Regardless of how far we travel with a composite video output, some sort of shielding is absolutely essential.

For short runs from board to board or inside equipment, tightly twisted conductors should be OK, as should properly guarded PC runs. Fully shielded cables should be used for interconnections between the TVT and the monitor or TV set, along with other long runs. As long as the total cable capacitance is less than 500 pF or so (this is around 18 feet of RG178-U miniature coax), the receiving end of the cable need not be terminated in a 72 or 100 Ohm resistor. When terminated cable systems are in use for long line runs or multiple outputs, they should be arranged to deliver the signal levels of Fig. 1 at their output under termination. Generally, terminated cable systems should be avoided as they need extra in the way of drivers and supply power.

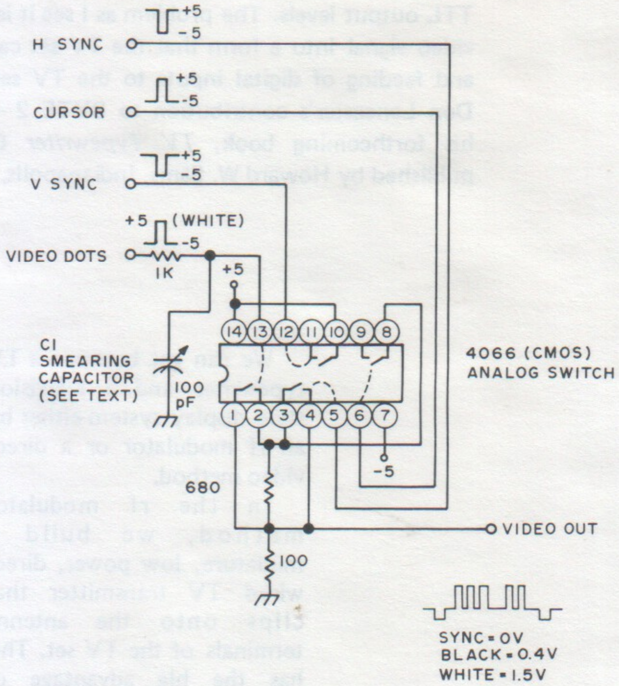
The exact width of the horizontal and vertical sync pulses isn't usually too important, so long as the shape and risetime of these pulses are independent of position control settings and power supply variations. One exception to this is when you're using a color receiver and a color display. Here, the horizontal sync pulse should be held closely to 5.1 microseconds, so the receiver's color burst sampling does in fact intercept a valid color burst. More on this later.

Intentional Smear

Fig. 2 shows us a typical composite video driver using a 4066 quad analog switch. It gives us a 100 Ohm output impedance and the proper signal levels. Capacitor C1 is used to purposely reduce the video rise and fall times. It is called a smearing capacitor.

Why would we want to further reduce the bandwidth and response of a TV system that's already hurting to begin with? In the case of a quality video monitor, we wouldn't. But if we're using an ordinary run-of-the-mill TV set, particularly one using rf entry, this capacitor can very much improve the display legibility and contrast. Why?

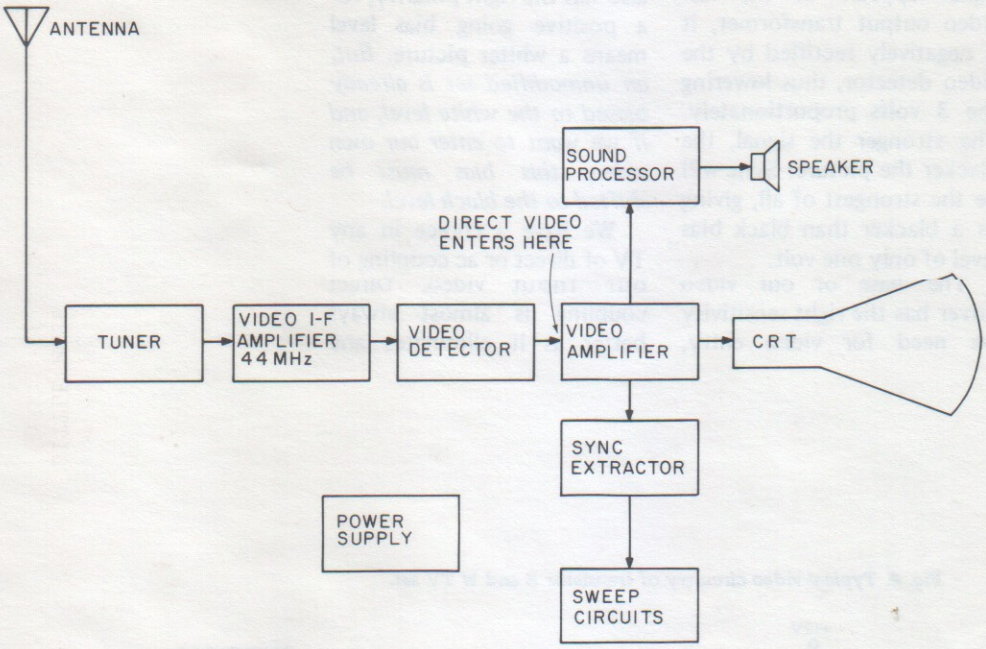
Fig. 2. Analog switch combiner generates composite video.



Because we are interested in getting the most legible character of the highest contrast we can. This is not necessarily the one having the sharpest dot rise and fall times. Many things interact to determine the upper video response of a TV display. These include the tuner settings and the i-f response and alignment, the video detector response, video peaking, the sound trap setting, rf cable reflections, and a host of other responses. Many of these stages are underdamped and will ring if fed too sharp a risetime input, giving us a ghosted, shabby, or washed out character. By reducing the video bandwidth going into the system, we can move the dot matrix energy lower in frequency, resulting in cleaner characters of higher contrast.

For most TV displays, intentional smearing will help the contrast, legibility, and overall appearance. The ultimate limit to this occurs when the dots overlap and become illegible. The

Fig. 3. Block diagram of typical B and W television.



optimum amount of intentional smear is usually the value of capacitance that is needed to just close the inside of a "W" presented to the display.

Adding a Video Input

Video inputs are easy to add to the average television set, provided you follow some reasonable cautions. First and foremost, you must have an accurate and complete schematic of the set to be modified, preferably a Sams Photofact or something similar. The first thing to check is the power supply on the set. If it has a power transformer and has the chassis properly safety isolated from the power line, it's a good choice for a TVT monitor. This is particularly true of recent small screen, solid state portable TV sets. On the other hand, if you have a hot chassis type with one side of the power line connected to the chassis, you should avoid its use if at all possible. If you must use this type of set, be absolutely certain to use one of the safety techniques outlined later in Fig. 8.

A block diagram of a typical TV set appears in Fig. 3. UHF or VHF signals picked up by the tuner are downconverted in frequency to a video i-f frequency of 44 MHz and then filtered and amplified. The output of the video i-f is transformer coupled to a video detector, most often a small signal germanium diode. The video detector output is filtered to remove the carrier and then routed to a video amplifier made up of one or more tubes or transistors.

At some point in the video amplification, the black and white signal is split three ways. First, a reduced bandwidth output routes sync pulses to the sync separator stage to lock the set's horizontal and vertical scanning to the video. A second bandpass output sharply filtered to 4.5 MHz extracts the FM sound subcarrier and routes this to a sound i-f amplifier for further processing. The third output is video, which is strongly amplified and then capacitively coupled to the cathode of the picture tube.

The gain of the video amplifier sets the contrast of the display, while the bias setting on the cathode of the picture tube (with respect to its grounded control grid) sets the display brightness. Somewhere in the video amplifier, further rejection of the 4.5 MHz sound subcarrier is usually picked up to minimize picture interference. This is called a sound trap. Sound traps can be a series resonant circuit to ground, a parallel resonant circuit in the video signal path, or simply part of the transformer that is picking off the sound for more processing.

The video detector output is usually around 2 volts peak to peak and usually subtracts from a white level bias setting. The stronger the signal, the more negative the swing, and the blacker the picture. Sync tips are blacker than black, helping to blank the display during retrace times.

Fig. 4 shows us the typical video circuitry of a transistor black and white television. Our basic circuit consists of a diode detector, a unity gain emitter follower, and a variable gain video output stage that is capacitively coupled to the picture tube. The cathode bias sets the brightness, while the video gain sets the contrast. Amplified signals for sync and sound are removed from the collector of the video driver by way of a 4.5 MHz resonant transformer for the sound and a low pass filter for the sync. A parallel resonant trap set to 4.5 MHz eliminates sound interference. Peaking coils on each stage extend the bandwidth by providing higher impedances and thus higher gain to high frequency video signals.

Note particularly the biasing of the video driver. A bias network provides us with a stable source of 3 volts. In the absence of input video, this 3 volts sets the white level of the display, as well as establishing proper bias for both stages. As an increasing signal appears at the last video output transformer, it is negatively rectified by the video detector, thus lowering the 3 volts proportionately. The stronger the signal, the blacker the picture. Sync will be the strongest of all, giving us a blacker than black bias level of only one volt.

The base of our video driver has the right sensitivity we need for video entry, accepting a maximum of a 2 volt peak to peak signal. It also has the right polarity, for a positive going bias level means a whiter picture. *But, an unmodified set is already biased to the white level, and if we want to enter our own video, this bias must be shifted to the black level.*

We have a choice in any TV of direct or ac coupling of our input video. Direct coupling is almost always better as it eliminates any

Fig. 4. Typical video circuitry of transistor B and W TV set.

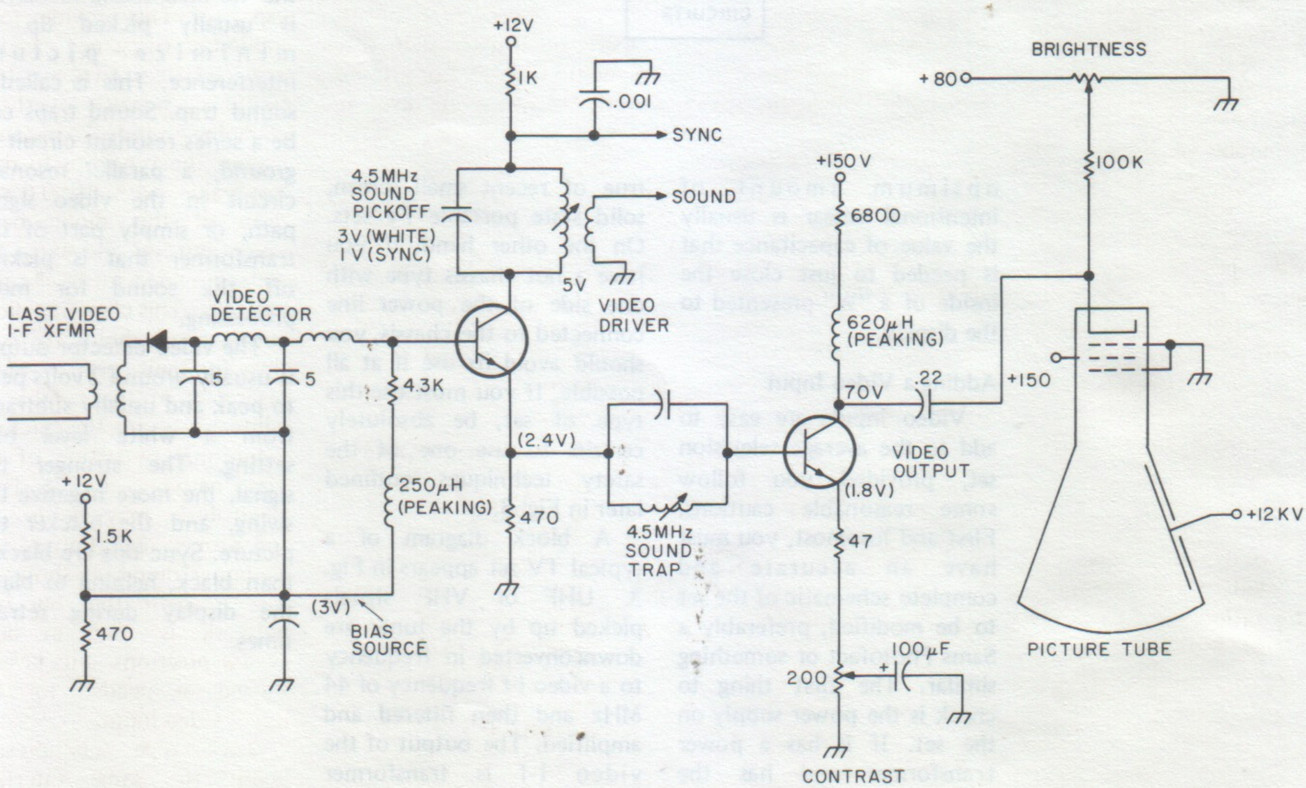
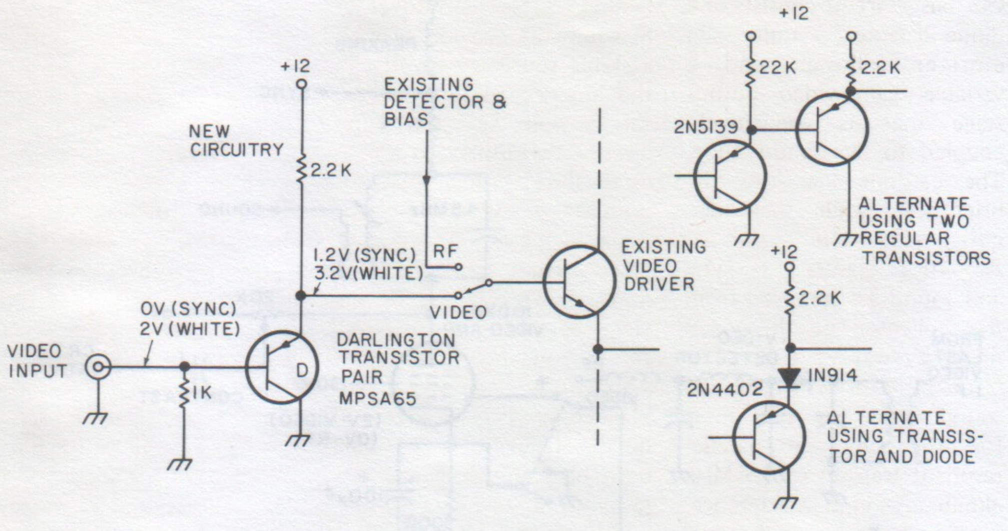


Fig. 5. Direct coupled video uses 1.2 volt offset of Darlington transistor as bias.



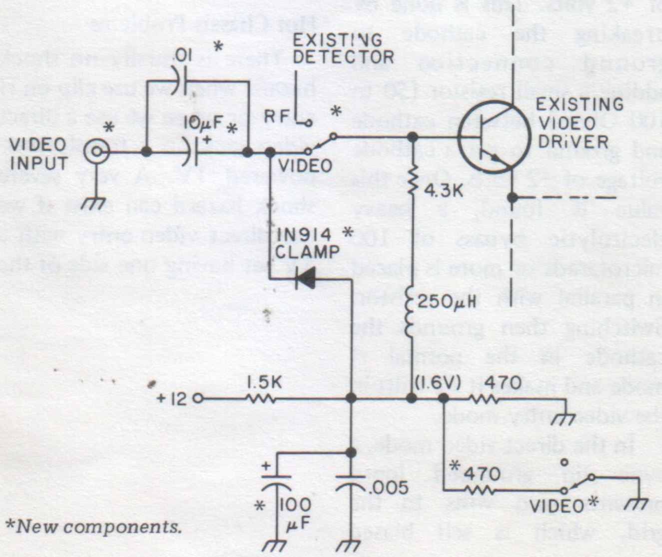
shading effects or any change of background level as additional characters are added to the screen. Fig. 5 shows how we can direct couple our video into a transistor black and white set. We provide a video input, usually a BNC or a phono jack, and route this to a PNP Darlington transistor or transistor pair, borrowing around 5 mils from the set's +12 volt supply. This output is routed to the existing video driver stage through a SPDT switch that either picks the video input or the existing video detector and bias network.

The two base-emitter diode drops in our Darlington transistor add up to a 1.2 volt positive going offset; so, in the absence of a video input or at the base of a sync tip, the video driver is biased to a blacker than black sync level of 1.2 volts. With a white video input of 2 volts, the video driver gets biased to its usual 3.2 volts of white level. Thus, our input transistor provides just the amount of offset we need to match the white and black bias levels of our video driver. Note that the old bias network is on the other side of the switch and does nothing in the video position.

Two other ways to offset our video input are to use two ordinary transistors connected in the Darlington configuration, or to use one transistor and a series diode to pick up the same amount of offset, as shown in Fig. 5. If more or less offset is needed, diodes or transistors can be stacked up further to pick up the right amount of offset.

The important thing is that the video driver ends up with the same level for white bias and for black bias in either position of the switch.

Fig. 6. Ac coupled video needs shift of bias to black level plus a clamping diode.

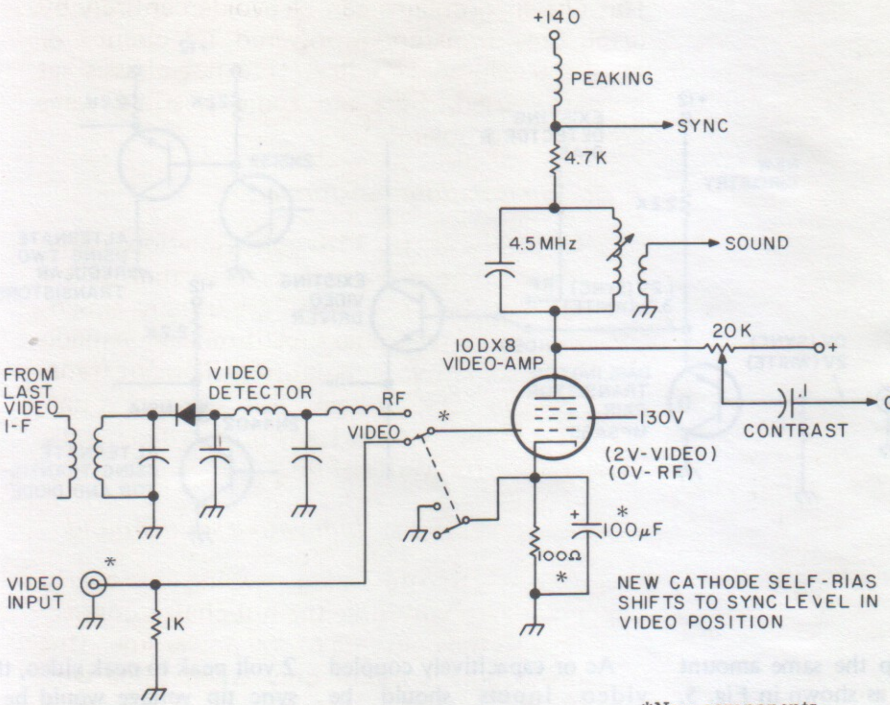


New components.

Ac or capacitively coupled video inputs should be avoided. Fig. 6 shows a typical circuit. The TV's existing bias network is lowered in voltage by adding a new parallel resistor to ground to give us a voltage that is 0.6 volts more positive than the blacker than black sync tip voltage. For instance, with a 3 volt white level, and 2 volt peak to peak video, the sync tip voltage would be 1 volt; the optimum bias is then 1.6 volts. Input video is capacitively coupled by a fairly large electrolytic capacitor in parallel with a good high frequency capacitor. This provides for a minimum of screen shading and still couples high frequency signals properly. A clamping diode constantly clamps the sync tips to their bias value, with the 0.6 volt drop of this diode being taken out by the extra 0.6 volts provided for in the bias network. This clamping diode automatically holds the sync tips to their proper value, regardless of the number of white dots in the picture. Additional bypassing of the bias network by a large electrolytic may be needed for proper operation of the clamping diode, as shown in Fig. 6. Note that our bias network is used in both switch positions — its level is shifted as needed for the direct video input.

Tube type sets present about the same interface problems as the solid state versions do. Fig. 7 shows a typical direct coupled tube interface. In the unmodified

Fig. 7. Direct coupled video added to tube type B and W television.



**New components.*

circuit, the white level is zero volts and the sync tip black level is minus two volts. If we can find a negative supply (scarce in tube type circuits), we could offset our video in the negative direction by two volts to meet these bias levels.

Instead of this, it is usually possible to self bias the video amplifier to a cathode voltage of +2 volts. This is done by breaking the cathode to ground connection and adding a small resistor (50 to 100 Ohms) between cathode and ground to get a cathode voltage of +2 volts. Once this value is found, a heavy electrolytic bypass of 100 microfarads or more is placed in parallel with the resistor. Switching then grounds the cathode in the normal rf mode and makes it +2 volts in the video entry mode.

In the direct video mode, a sync tip grounded input presents zero volts to the grid, which is self biased minus two volts with respect to the cathode. A white level presents +2 volts to the grid, which equals zero volts grid to cathode.

Should there already be a self bias network on the cathode, it is increased in value as needed to get the black rather than white level bias in the direct video mode.

Hot Chassis Problems

There is usually no shock hazard when we use clip-on rf entry or when we use a direct video jack on a transformer-powered TV. A very severe shock hazard can exist if we use direct video entry with a TV set having one side of the power line connected to the chassis. Depending on which way the line cord is plugged in, there is a 50-50 chance of the hot side of the power line being connected directly to the chassis.

Hot chassis sets, particularly older, power hungry tube versions, should be avoided entirely for direct video entry. If one absolutely must be used, some of the suggestions of Fig. 8 may ease the hazard. These include using an isolation transformer, husky back-to-back filament transformers, three wire power systems, optical coupling of the video input, and total package isolation. Far and away the best route is simply never to attempt direct video entry onto a hot chassis TV.

Making the Conversion

Fig. 9 sums up how we modify a TV for direct video entry. Always have a complete schematic on hand, and use a transformer style TV set if at all possible. Late models, small screen, medium to high quality solid state sets are often the best display choice. Avoid using junk sets, particularly very old ones. Direct coupling of video is far preferable to ac capacitor coupling. Either method has to maintain the black and white bias levels on the first video amplifier stage. A shift of the first stage quiescent bias from normally white to normally black is also a must. Use short, shielded leads between the video input jack and the rest of the circuit. If a changeover switch is used, keep it as close to the rest of the video circuitry as you possibly can.

Extending Video and Display Bandwidth

By using the direct video input route, we eliminate any bandwidth and response restrictions of an rf modulator, the tuner, video i-f strip, and the video detector filter. Direct video entry should bring us to a 3 MHz bandwidth for a color set and perhaps 3.5 MHz for a black and white model, unless we are using an extremely bad set. The resultant 6 to 7 million dot per second rate is adequate for short character lines of 32, 40, and possibly 48 characters per line. But the characters will smear and be illegible if we try to use longer line lengths and premium (lots of dots) character generators on an ordinary TV. Is there anything we can do to the set to extend the video bandwidth and display response for these longer line lengths?

In the case of a color TV, the answer is probably no. The video response of a color set is limited by an essential delay line and an essential 3.58 MHz trap. Even if we were willing to totally separate the chrominance and luminance channels, we'd still be faced with an absolute limit set by the number of holes per horizontal line in the shadow mask of the tube. This explains why video color displays are so expensive and so rare. Later on, we'll look at what's involved in adding color to the shorter line lengths.

With a black and white TV, there is often quite a bit

Fig. 8. Getting Around a Hot Chassis Problem.

Hot chassis problems can be avoided entirely by using only transformer-powered TV circuits or by using clip-on rf entry. If a hot chassis set must be used, here are some possible ways around the problem:

1. Add an isolation transformer.

A 110 volt to 110 volt isolation transformer whose wattage exceeds that of the set may be used. These are usually expensive, but a workable substitute can be made by placing two large surplus filament transformers back to back. For instance, a pair of 24 volt, 4 Amp transformers can handle around 100 Watts of set.

2. Use a three wire system with a solid ground.

Three prong plug wiring, properly polarized, will force the hot chassis connection to the cold side of the power line. This protection is useful only when three wire plugs are used in properly wired outlets. A severe shock hazard is reintroduced if a user elects to use an adaptor or plugs the system into an unknown or improperly wired outlet. The three wire system should NOT be used if anyone but yourself is ever to use the system.

3. Optically couple the input video.

Light emitting diode-photocell pairs are low in cost and can be used to optically couple direct video, completely isolating the video input from the hot chassis. Most of these optoelectronic couplers do not have enough bandwidth for direct video use; the Litronix IL-100 is one exception. Probably the simplest route is to use two separate opto-isolators, one for video and one for sync, and then recombine the signals inside the TV on the hot side of the circuit.

4. Use a totally packaged and sealed system.

If you are only interested in displaying messages and have no other input/output devices, you can run the entire circuit hot chassis, provided everything is sealed inside one case and has no chassis-to-people access. Interface to teletypes, cassettes, etc., cannot be done without additional isolation, and servicing the circuit presents the same shock hazards that servicing a hot chassis TV does.

we can do to present long lines of characters, depending on what set you start out with and how much you are willing to modify the set.

The best test signal you can use for bandwidth extension is the dot matrix data you actually want to display, for the frequency response, time delay, ringing, and overshoot all get into the act. What we want to end up with is a combination that gives us reasonably legible characters.

A good oscilloscope (15 MHz or better bandwidth) is very useful during bandwidth extension to show where the signal loses its response in the circuit. At any time during the modification process, there is usually one response bottleneck. This, of course, is what should be attacked first. Obviously the better a TV you start with, the easier will be the task. Tube type gutless wonders, particularly older ones, will be much more difficult to work with than with a modern, small screen, quality solid state portable.

Several of the things we can do are watching the control settings, getting rid of the sound trap, minimizing circuit strays, optimizing spot size, controlling peaking, and shifting to higher current operation. Let's take a look at these in turn.

Control Settings

Always run a data display at the lowest possible contrast and using only as much brightness as you really need. In many circuits, low contrast means a lower video amplifier gain, and thus less of a gain-bandwidth restriction.

Eliminate the Sound Trap

The sound trap adds a notch at 4.5 MHz to the video response. If it is eliminated or switched out of the circuit, a wider video bandwidth automatically

Fig. 9. How to Add a Direct Video Input to a TV Set.

1. Get an accurate and complete schematic of the set — either from the manufacturer's service data or a Photofact set. **Do not try adding an input without this schematic!**

2. Check the power supply to see if a power transformer is used. If it is, there will be no shock hazard, and the set is probably a good choice for direct video use. If the set has one side of the power line connected to the chassis, a severe shock hazard exists, and one of the techniques of Fig. 8 should be used. **Avoid the use of hot chassis sets.**

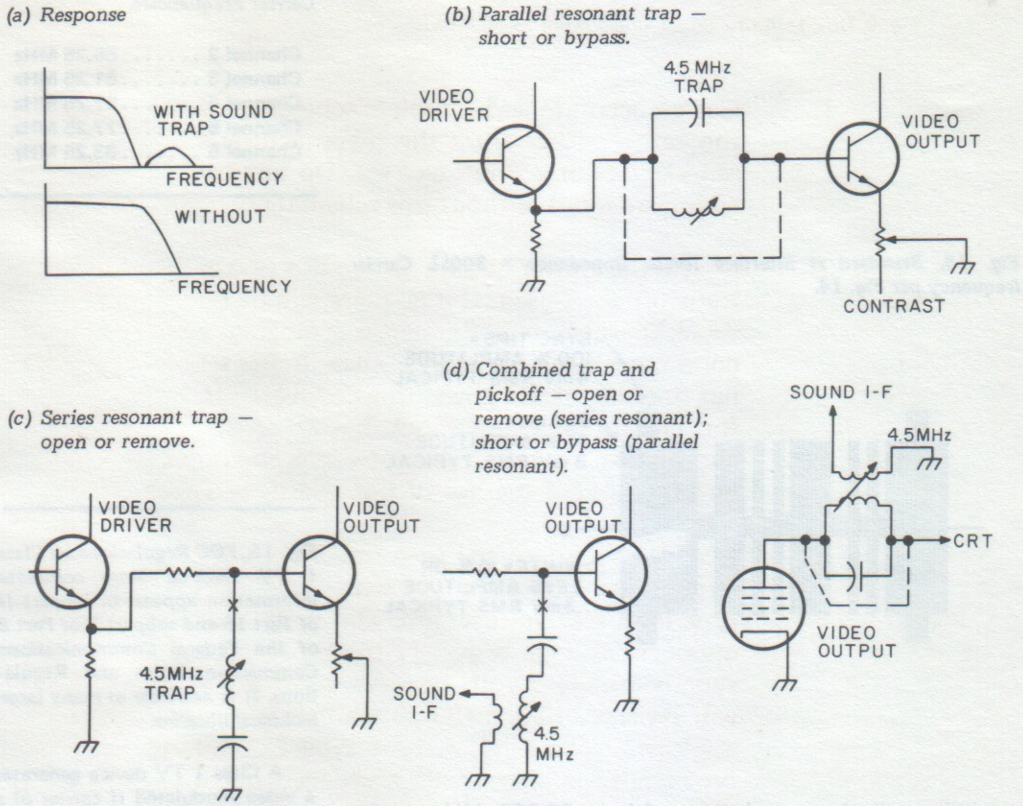
3. Find the input to the first video amplifier stage. Find out what the white level and sync level bias voltages are. The marked or quiescent voltage is usually the white level; sync is usually 2 volts less. A transistor TV will typically have a +3 volt white level and a +1 volt sync level. A tube type TV will typically have a zero volt white level and a -2 volt sync level.

4. Add a changeover switch using minimum possible lead lengths. Add an input connector, either a phono jack or the premium BNC type connector. Use shielded lead for interconnections exceeding three inches in length.

5. Select a circuit that couples the video and biases the first video amplifier stage so that the white and sync levels are preserved. For transistor sets, the direct coupled circuits of Fig. 5 may be used. For tube sets, the circuit of Fig. 7 is recommended. Avoid the use of ac coupled video inputs as they may introduce shading problems and changes of background as the screen is filled.

6. Check the operation. If problems with contrast or sync tearing crop up, recheck and adjust the white and sync input levels to match what the set uses during normal rf operation. Note that the first video stage must be biased to the white level during rf operation and to the sync level for direct video use. The white level is normally two volts more positive than the sync level.

Fig. 10. Removing the sound trap can extend video bandwidth.



results. Fig. 10 shows us the response changes and the several positions for this trap. Generally, series resonant traps are opened and parallel resonant traps are shorted or bypassed through suitable switching or outright elimination. The trap has to go back into the circuit if the set is ever again used for ordinary program reception. Sometimes simply backing the slug on the trap all the way out will improve things enough to be useful.

Minimizing Strays

One of the limits of the video bandwidth is the stray capacitance both inside the video output stage and in the external circuitry. If the contrast control is directly in the signal path and if it has long leads going to it, it may be hurting the response. If you are using the TV set exclusively for data display, can you rearrange the control location and simplify and shorten the video output to picture tube interconnections?

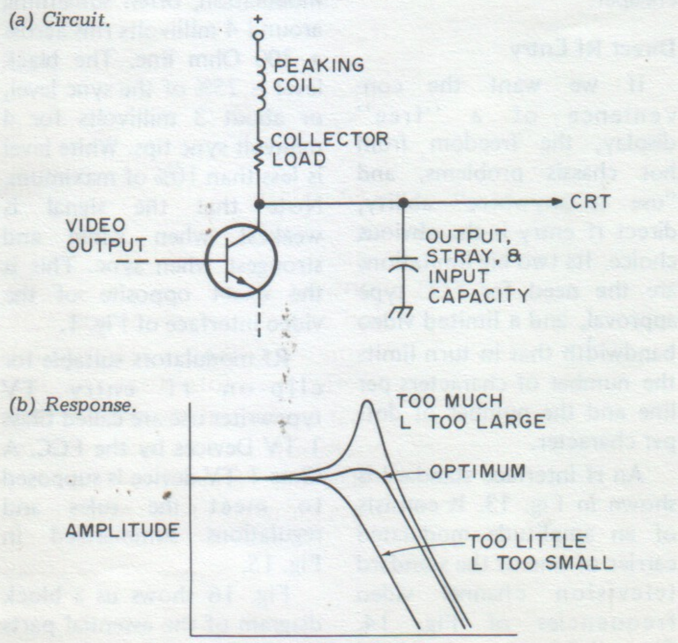
Additional Peaking

Most TV sets have two peaking networks. The first of these is at the video detector output and compensates for the vestigial sideband transmission signal that makes sync and other low frequency signals double the amplitude of the higher frequency ones. The second of these goes to the collector or plate of the video output stage and raises the circuit impedance and thus the effective gain for very high frequencies. Sometimes you can alter this second network to favor dot presentations. Fig. 11 shows a typical peaking network and the effects of too little or too much peaking. Note that the stray capacitance also enters into the peaking, along with the video amplifier output capacitance and the picture tube's input capacitance. Generally, too little peaking will give you low contrast dots, while too much will give you sharp dots, but will run dots together and shift the more continuous portions of the characters objectionably. Peaking is changed by increasing or decreasing the series inductor from its design value.

Running Hot

Sometimes increasing the operating current of the video output stage can increase the system bandwidth — IF this stage is in fact the limiting response, IF the power supply can handle the extra current, IF the stage isn't already parked at its gain-bandwidth peak, and IF the extra heat can be gotten rid of without burning anything up. Usually, you can try adding a resistor three times the plate or collector load resistor in parallel, and see if it increases bandwidth by 1/3. Generally, the higher the current, the wider the bandwidth, but watch

Fig. 11. Adjusting the peaking coil can extend video response.



carefully any dissipation limits. Be sure to provide extra ventilation and additional heatsinking, and check the power supply for unhappiness as well. For major changes in operating current, the emitter resistors and other biasing components should also be proportionately reduced in value.

Spot Size

Even with excellent video bandwidth, if you have an out-of-focus, blooming, or changing spot size, it can completely mask character sharpness. Spot size ends up the ultimate limit to resolution, regardless of video bandwidth.

Once again, brightness and contrast settings will have a profound effect, with too much of either blooming the spot. Most sets have a focus jumper in which ground or a positive voltage is selected. You can try intermediate values of voltage for maximum sharpness. Extra power supply filtering can sometimes minimize hum and noise modulation of the spot.

Anything that externally raises display contrast will let you run with a smaller beam current and a sharper spot. Using circularly polarized filters, graticule masks, or simple colored filters can minimize display washout from ambient lighting. Fig. 12 lists several sources of material for contrast improvement. Much of this is rather expensive, with pricing from $10 to $25 per square foot being typical. Simply adding a hood and positioning the display away from room lighting will also help and is obviously much cheaper.

Fig. 12. Contrast Enhancing Filter Materials.

Circularly polarized filters:

Polaroid Corp.
Cambridge MA 02139

Anti-reflection filters:

Panelgraphic Corp.
10 Henderson Dr.
West Caldwell NJ 07006

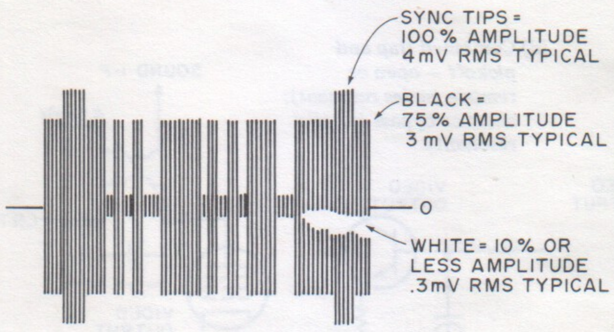
Light control film:

3M Visual Products Div.
3M Center
St. Paul MN 55101

Acrylic plexiglas filter sheets:

Rohm and Haas
Philadelphia PA 19105

Fig. 13. Standard rf interface levels. Impedance = 300Ω. Carrier frequency per Fig. 14.



Direct Rf Entry

If we want the convenience of a "free" display, the freedom from hot chassis problems, and "use it anywhere" ability, direct rf entry is the obvious choice. Its two big limitations are the need for FCC type approval, and a limited video bandwidth that in turn limits the number of characters per line and the number of dots per character.

An rf interface standard is shown in Fig. 13. It consists of an amplitude modulated carrier of one of the standard television channel video frequencies of Fig. 14. Channel 2 is most often used with a 55.250 MHz carrier frequency, except in areas where a local commercial Channel 2 broadcast is intolerably strong. Circuit cost, filtering problems, and stability problems tend to increase with increasing channel number.

The sync tips are the strongest part of the signal, representing 100% modulation, often something around 4 millivolts rms across a 300 Ohm line. The black level is 75% of the sync level, or about 3 millivolts for 4 millivolt sync tips. White level is less than 10% of maximum. Note that the signal is weakest when white and strongest when sync. This is the exact opposite of the video interface of Fig. 1.

Rf modulators suitable for clip-on rf entry TV typewriter use are called Class 1 TV Devices by the FCC. A Class 1 TV device is supposed to meet the rules and regulations summarized in Fig. 15.

Fig. 16 shows us a block diagram of the essential parts of a TV modulator. We start

Fig. 14. Television Picture Carrier Frequencies.

Channel 2	**55.25 MHz**
Channel 3	**61.25 MHz**
Channel 4	**67.25 MHz**
Channel 5	**77.25 MHz**
Channel 6	**83.25 MHz**

Fig. 15. FCC Regulations on Class 1 TV Devices. More complete information appears in subpart H of Part 15 and subpart F of Part 2 of the Federal Communications Commission Rules and Regulations. It is available at many large technical libraries.

A Class 1 TV device generates a video modulated rf carrier of a standard television channel frequency. It is directly connected to the antenna terminals of the TV set.

The maximum rms rf voltage must be less than 6 millivolts using a 300 Ohm output line.

The maximum rf voltage on any frequency more than 3 MHz away from the operating channel must be more than 30 dB below the peak in-channel output voltage.

An antenna disconnect switch of at least 60 dB attenuation must be provided.

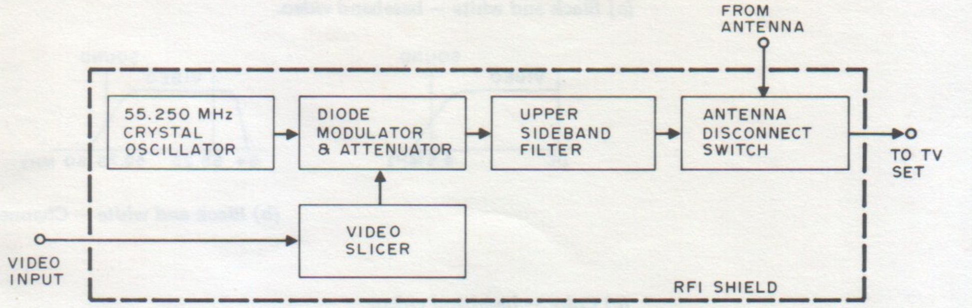
No user adjustments are permitted that would exceed any of the above specifications.

Residual rf radiation from case, leads and cabinet must be less than 15 microvolts per meter.

A Class 1 TV device must not interfere with TV reception.

Type approval of the circuit is required. A filing fee of $50 and an acceptance fee of $250 is involved.

Fig. 16. Block diagram of rf modulator.



with a stable oscillator tuned to one of the Fig. 14 frequencies. A crystal oscillator is a good choice, and low cost modules are widely available. The output of this oscillator is then amplitude modulated. This can be done by changing the bias current through a silicon small signal diode. One milliampere of bias current makes the diode show an ac and rf impedance of 26 Ohms. Half a mil will look like 52 Ohms, and so on. The diode acts as a variable resistance attenuator in the rf circuit, whose bias is set and changed by the video circuit.

Since diode modulators are non-linear, we can't simply apply a standard video signal to them and get a standard rf signal out. A differential amplifier circuit called a video slicer may be used to compensate for this non-linearity. The video slicer provides three distinct currents to the diode modulator. One of these is almost zero for the white level, while the other two provide the black and sync levels. A contrast control that sets the slicing level lets you adjust the sync tip height with respect to the black level. The video slicer also minimizes rf getting back into the video. An attenuator to reduce the size of the modulated signal usually follows the diode modulator.

An upper side band filter removes most of the lower sideband from the AM modulated output, giving us a vestigial sideband signal that stays inside the channel band limits. This same filter eliminates second harmonic effects and other spurious noise. The filter's output is usually routed to an antenna disconnect switch and the TV's antenna terminals. A special switch is needed to provide enough isolation.

Some of the actual circuitry involved is shown in Fig. 17. The video slicer consists of a pair of high gain, small signal NPN transistors, while the oscillator is a commercially available module.

Rf entry systems always must be direct coupled to the antenna terminals of the set and should never provide any more rf than is needed for a minimum snow-free picture. They should be permanently tuned to a single TV channel. Under no circumstances should an antenna or cable service hookup remain connected to the set during TVT use, nor should radiation rather than a direct rf cable connection ever be used.

Color Techniques

We can add a full color capability to a TV typewriter system fairly easily and cheaply – provided its usual black and white video dot rate is low enough in frequency to be attractively displayed on an ordinary color TV. Color may be used to emphasize portions of a message, to attract attention, as part of an electronic game, or as obvious added value to a graphics display. Color techniques work best on TV typewriter systems having a horizontal frequency very near 15,735 Hertz.

All we basically have to do is generate a subcarrier sine wave to add to the video output. The phase of this subcarrier (or its time delay) is shifted with respect to what the phase was immediately after each horizontal sync pulse to generate the various colors.

Fig. 18 shows us the differences between normal color and black and white operation. Black and white baseband video is some 4 MHz wide and has a narrow 4.5 MHz sound subcarrier. The video is amplitude modulated, while the sound is narrow band frequency

Fig. 17. Channel two oscillator, modulator, video slicer and attenuator. R sets output level.

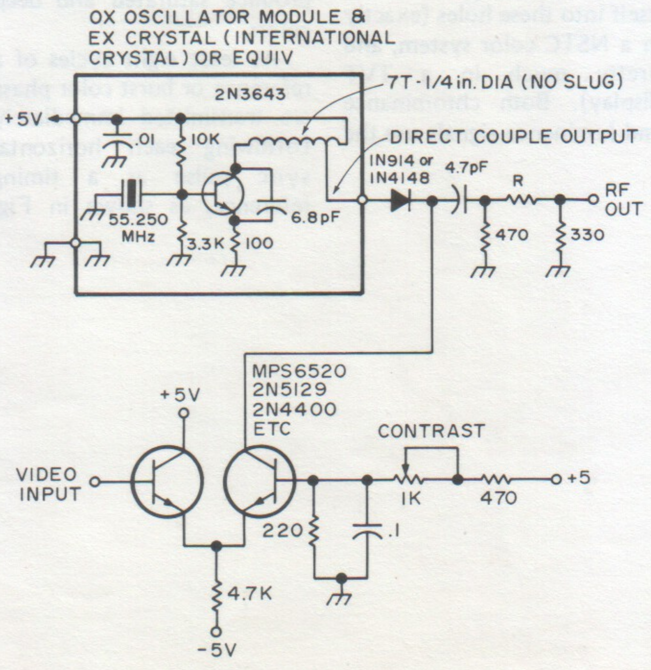
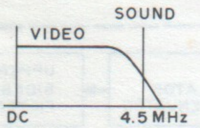
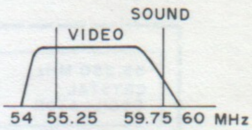


Fig. 18. Differences between color and black and white spectra.

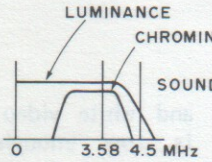
(a) Black and white – baseband video.

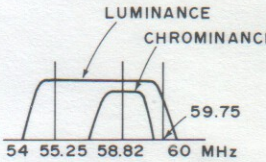




(b) Black and white – Channel two rf.

(c) Color – baseband video.





(d) Color – Channel two rf.

modulated. This translates up to a 6 MHz rf channel with a vestigial lower sideband as shown in Fig. 18(b).

To generate color, we add a new pilot or subcarrier at a magic frequency of 3.579545 MHz – see Fig. 18(c). What was the video is now called the luminance, and is the same as the brightness in a black and white system. The new subcarrier and its modulation is called the chrominance signal and determines what color gets displayed and how saturated the color is to be.

Since the black and white information is a sampled data system that is scanned at the vertical and horizontal rates, there are lots of discrete holes in the video spectrum that aren't used. The color subcarrier is designed to stuff itself into these holes (exactly in a NSTC color system, and pretty much in a TVT display). Both chrominance and luminance signals use the same spectral space, with the one being where the other one isn't, overlapping comb style.

The phase or relative delay of the chrominance signal with respect to a reference determines the instantaneous color, while the amplitude of this signal with respect to the luminance sets the saturation of the color. Low amplitudes generate white or pastel shades, while high amplitudes of the chrominance signal produce saturated and deep colors.

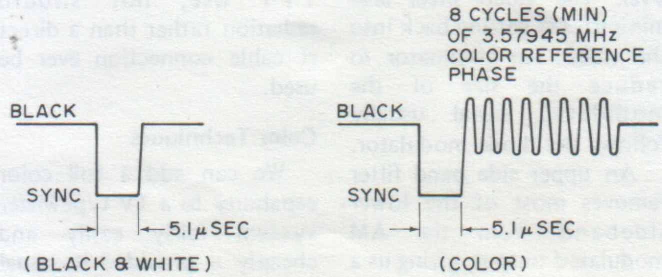
At least eight cycles of a reference or burst color phase are transmitted immediately following each horizontal sync pulse as a timing reference, as shown in Fig. 19. The burst is around 25% of maximum amplitude, or about the peak to peak height of a sync pulse.

The TV set has been trained at the factory to sort all this out. After video detection, the set splits out the chrominance channel with a bandpass amplifier and then synchronously demodulates it with respect to an internal 3.58 MHz reference. The phase of this demodulation sets the color and the amplitude sets the saturation by setting the ratios of electron beam currents on the picture tube's red, blue and green guns.

Meanwhile, the luminance channel gets amplified as brightness style video. It is delayed with a delay line to make up for the time delay involved in the narrower band color processing channel. It is then filtered with two traps – the 4.5 MHz sound trap, and a new trap to get rid of any remaining 3.58 MHz color subcarrier that's left. The luminance output sets the overall brightness by modulating the cathodes of all three color guns simultaneously.

Just after each horizontal sync pulse, the set looks for the reference burst and uses this reference in a phase

Fig. 19 Adding a color reference burst to the back porch of the horizontal sync pulses.



J3 Keyboard Connector (between U64 and U65)

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	+5v	12	+5v
3	Kbd Data Ready	13	Restart
4	Break	14	Local
5	Kbd Data Ø	15	KBd Data 4
6	Kbd Data 1	16	KBd Data 5
7	Kbd Data 2	17	KBD Data 6
8	Kbd Data 3	18	KBD Data 7
9	+5v	19	+5v
10	ground	20	ground

J4 Display Expansion Connector (between U28, 29)

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	N.C.	12	N.C.
3	Char. addr. 4	13	Dot Clock, 14.318MHz
4	Character clock	14	Composite sync. out
5	Char. addr. Ø	15	TTL Serial Data Out
6	Char. addr. 1	16	Composite blanking out
7	Char. addr. 2	17	Scan advance out
8	Char. addr. 3	18	Char. addr. 5
9	N.C.	19	N.C.
10	ground	20	ground

J5 Personality Module Edge Connector

pin no.	Signal name	pin no.	Signal name
B15	Ground	A15	Ground
B14	+5VDC	A14	+5VDC
B13	Addr. 9	A13	Addr. Ø
B12	Addr. 8	A12	Addr. 4
B11	Addr. 7	A11	Addr. 3
B10	INT Bus Ø	A10	Addr. 2
B9	INT Bus 1	A9	Addr. 1
B8	INT Bus 2	A8	Addr. 5
B7	INT Bus 3	A7	Addr. 6
B6	INT Bus 4	A6	C4
B5	INT Bus 5	A5	CØ
B4	Program Ø	A4	INT Bus 6
B3	Program 1	A3	INT Bus 7
B2	Program 2	A2	-12VDC
B1	Program 3	A1	+12VDC

J6 Audio Out for CUTS Cassette Interface: Mini-phone jack at rear panel

J7 Audio In for CUTS Cassette Interface: Mini-phone jack at rear panel

J8 Tape Motor Control 1: (See output port FA, bit 7) Sub-mini jack at rear panel

J9 Tape Motor Control 2: (See output port FA, bit 6) Sub-mini jack at rear panel

J10 DC Power Connector, Sol-PC

Pin
Ground
+5VDC
-12 VDC
+12 VDC
-12 VDC
+5 VDC
Ground

S-100 Bus Definitions

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	+8V	+8 Volts	Unregulated voltage on bus, supplied to PC boards and regulated to 5V supplied by Sol-20 supply
2	-16V	-16 Volts	Positive unregulated voltage supplied by Sol-20 power supply
3	XRDY	EXTERNAL READY	External ready input to CPU ready circuitry
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12	XRDY2	EXTERNAL READY #2	not used by Sol-PC
13 to 17	TO BE DEFINED		
18	$\overline{\text{STAT DSB}}$	STATUS DISABLE	-Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	COMMAND/CONTROL DISABLE	-Allows the buffers for the 6 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	-not used by Sol-PC electronics
21	SS	SINGLE STEP	-not used by Sol-PC
22	$\overline{\text{ADD DSB}}$	ADDRESS DISABLE	-Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSB}}$	DATA OUT DISABLE	-Allows the buffers for the 8 data output lines to be tri-stated
24	Ø2	PHASE 2 CLOCK	
25	Ø1	PHASE 1 CLOCK	
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle.

S-100 Bus Definitions-continued

PIN NUMBER	SYMBOL	NAME	FUNCTION
27	PWAIT	WAIT	-Processor command/control signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle
28	PINTE	INTERRUPT ENABLE	-Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited.
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	(MSB)
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DIO1	Data In/Out line #1	same as pin 94
36	DIOØ	Data In/Out line #0	same as pin 95
37	A10	Address Line #10	
38	DIO4	Data In/Out Line #4	same as pin 91
39	DIO5	Data In/Out Line #5	same as pin 92
40	DIO6	Data In/Out Line #6	same as pin 93
41	DIO2	Data In/Out Line #2	same as pin 88
42	DIO3	Data In/Out Line #3	same as pin 89
43	DIO7	Data In/Out Line #7	same as pin 90
44	SM1	MACHINE CYCLE 1	-Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUTPUT	-Status output signal that indicates the address bus contains the address of an output device and the data bus will contain the ouput data when PWR is active
46	SINP	INPUT	-Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMORY READ	-Status output signal that indicates the data bus will be used to read memory data
48	SHLTA	HALT ACKNOWLEDGE	- Status output signal that acknowledges a HALT instruction
49	CLOCK	CLOCK	- Inverted output of the Ø2 CLOCK
50	GND	GROUND	
51	+8V	+8 Volts	Unregulated input to 5 volt regulators supplied by Sol-20 power supply
52	-16V	-16 Volts	Negative unregulated voltage supplied by Sol-20 power supply

S-100 Bus Definitions-continued

PIN NUMBER	SYMBOL	NAME	FUNCTION
53	SSWI	SENSE SWITCH INPUT	not used by Sol
54	EXT CLR	EXTERNAL CLEAR	not used by Sol-PC electronics
55	RTC	REAL TIME CLOCK	not used by Sol-PC electronics
56	STSTB	STATUS STROBE	not used by Sol
57	DIGI	DATA INPUT GATE #1	When low forces PDBINS low and forces CPU input multiplexers to the DIO bus. During CPU DBIN cycle, disables CPU DIO bus drivers
58	FRDY	FRONT PANEL READY	-When low disables MWRITE driver
59 to 64	TO BE DEFINED		
65	MREQ	MEMORY REQUEST	- Z 80 signal not used by Sol-PC electronics
66	REF	REFRESH	- Z 80 signal not used by Sol-PC electronics
67	PHANTOM	PHANTOM DISABLE	-Output from CPU section used to disable RAM or ROM during power on initialization program execution
68	MWRITE	MEMORY WRITE	-Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus
69	PS	PROJECT STATUS	-not used by Sol-PC electronics
70	PROT	PROTECT	-not used by Sol-PC electronics
71	RUN	RUN	-not used by Sol-PC electronics
72	PRDY	PROCESSOR READY	-Memory and I/O input to the CPU Board wait circuitry
73	PINT	INTERRUPT REQUEST	- The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	PHOLD	HOLD	-Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle
75	PRESET	RESET	-Processor command/control input; while activated, the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	-Processor command/control output; provides a signal to indicate the beginning of each machine cycle
77	PWR	WRITE	-Processor command/control output; used for memory write or I/O output control. Data on the data bus is stable while the PWR is active
78	PDBIN	DATA BUS IN	-Processor command/control output; indicates to external circuits that the data bus is in the input mode

S-100 Bus Definitions-continued

PIN NUMBER	SYMBOL	NAME	FUNCTION
79	A0	Address Line #0	(LSB)
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DI02	Data In/Out Line #2	same as pin 41
89	DI03	Data In/Out Line #3	same as pin 42
90	DI07	Data In/Out Line #7	same as pin 43
91	DI04	Data In/Out Line #4	same as pin 38
92	DI05	Data In/Out Line #5	same as pin 39
93	DI06	Data In/Out Line #6	same as pin 40
94	DI01	Data In/Out Line #1	same as pin 35
95	DIØ	Data In/Out Line #0	same as pin 36
96	SINTA	INTERRUPT ACKNOWLEDGE	-Status output signal; acknowledges signal for INTERRUPT request
97	$\overline{SWO}$	$\overline{WRITE\ OUT}$	-Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	-Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{POC}$	$\overline{POWER\text{-}ON\ CLEAR}$	
100	GND	GROUND	

SWITCH FUNCTION DEFINITION -- Display Ctrl---Schematic Drawing #4

Switch No.	Mnemonic	Function ON	Function OFF
S1-1	RST	Restart to Zero	RUN (Dwg. #1)
S1-2	not used		
S1-3	BLANK	Blank Ctrl Characters	Display Ctrl Char.
S1-4	Polarity		
S1-5	BLINK	Blinking cursor	*Solid or NO cursor
S1-6	SOLID	Solid cursor	*Blinking or NO cursor

*NO cursor if S1-5 and S1-6 are off at same time.
Both switches should not be on at the same time.

Drawing #3 -- Sense Switch

Switch No.	Mnemonic	Function ON	OFF	
S2-1	SSWØ	LSB, data bit	Ø=LO	HI
S2-2thruS2-7		etc.	LO	HI
S2-8	SSW7	MSB data bit 7	LO	HI

SERIAL I/O BAUD RATE SWITCH -- Schematic Drawing #3

Switch No.	Mnemonic	Function ON	Function OFF
S3-1	75	75 BAUD	* Do not turn more than one switch on at a time
S3-2	11	110 BAUD	
S3-3	15	150 BAUD	
S3-4	30	300 BAUD	
S3-5	60	600 BAUD	
S3-6	12	1200 BAUD	
S3-7	24/48	2400 or 4800(normally 2400 if not jumpered K to M)	
S3-8	96	9600 BAUD	

SERIAL I/O CONTROL -- Schematic Drawing #3

Switch No.	Mnemonic	ON	OFF
S4-1	PS	Parity even	Parity odd (if S4-5 on)
S4-2	WLS 1	Data word length	8bits 7bits 6bits 5bits: ON ON OFF OFF
S4-3	WLS 2		ON OFF ON OFF
S4-4	SBS	1 stop bit	2 stop bits (1.5 if 5bits/word)
S4-5	PI	Parity	No parity
S4-6	F/$\overline{H}$	Half duplex	Full duplex

MEMORY ALLOCATION: ON CARD

Hexidecimal Address	Function
CØØØ - C7FF	Personality Module ROM or PROM (2048 words)
C8ØØ - CBFF	System RAM (1024 words)
CCØØ - CFFF	Display RAM Memory (1024 characters)

ON CARD INPUT PORT ALLOCATION

Hexidecimal Port Address	Function
F8	Status, Serial Comm. channel
F9	Serial Communication Channel Data
FA	Aux. Status, Cassette tape interface, parallel I/O, keyboard input
FB	Audio Cassette (CUTS) Data
FC	Keyboard Data (from J3)
FD	Parallel Port Data (from J2)
FE	Display Status
FF	Sense Switch (S2-1 thru S2-8)

OUTPUT PORTS

Hex Port Address	Function
F8	Control, Serial Comm. Channel
F9	Data, Serial Comm. Channel
FA	Control, Parallel I/O, CUTS Cassette I/O
FB	Data, CUTS audio cassette Interface
FC	Alarm (optional)
FD	Data, Parallel output Data channel
FE	Scroll control, Display Section
FF	not used in Sol-PC

STATUS PORT INPUT BIT ASSIGNMENTS

PORT F8 (STATUS, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SCD	Serial Carrier Detect (EIA)	1 carrier
1	SDSR	Serial Data Set Ready (EIA)	Ø link ok
2	SPE	Serial Parity Error	1 error
3	SFE	Serial Framing Error	1 error
4	SOE	Serial Overrun Error	1 error
5	SCTS	Serial Clear to Send (EIA)	Ø clear
6	SDR	UART Serial Data Ready	1 ready
7	STBE	UART Serial Transmit Buffer Empty	1 empty

PORT FA (AUX. STATUS, CASSETTE TAPE INTERFACE, PARALLEL I/O, KEYBOARD INPUT)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	KDR	Keyboard Data Ready	Ø ready
1	PDR	Parallel Data Ready	Ø ready
2	PXDR	Parallel eXternal Device Ready	Ø ready
3	TFE	Tape Framing Error	1 error
4	TOE	Tape Overrun Error	1 error
5	not used		
6	TDR	Tape Data Ready	1 ready
7	TTBE	Tape Transmitter Buffer Empty	1 empty

PORT FE (DISPLAY STATUS)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SOK	Scroll OK; ¼ sec timeout after scroll	Ø time complete

CONTROL PORT OUTPUT BIT ASSIGNMENTS

PORT F8 (CONTROL, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
4	SRTS	Serial Request to Send	1 request

PORT FA (CONTROL, PARALLEL I/O, CUTS CASSETTE I/O)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
3	PIE	Parallel Input Enable	1 pin 3 J2 low
4	PUS	Parallel Unit Select	0 pin 14 J2 low
5	TBR	Tape Baud Rate (300/1200)	0 1200 Baud
6	TT2	Tape Transport 2	0 run tape
7	TT1	Tape Transport 1	0 run tape

PORT FE (SCROLL CONTROL, DISPLAY SECTION)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø - 3	BDLA	Beginning Display Line Absolute address	4-bit data nybble
4 - 7	FDSP	First Displayed Line Screen Position	4-bit data nybble

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CONNECTOR DESIGNATION

J1	Serial data
J2	Parallel Data
J3	Keyboard
J4	Display Expansion
J5	ROM Personality Module
J6	Cassette Tape Audio Out
J7	Cassette Tape Audio In
J8	Tape Motor 1
J9	Tape Motor 2
J10	PC Power
J11	S-100 Bus Expansion