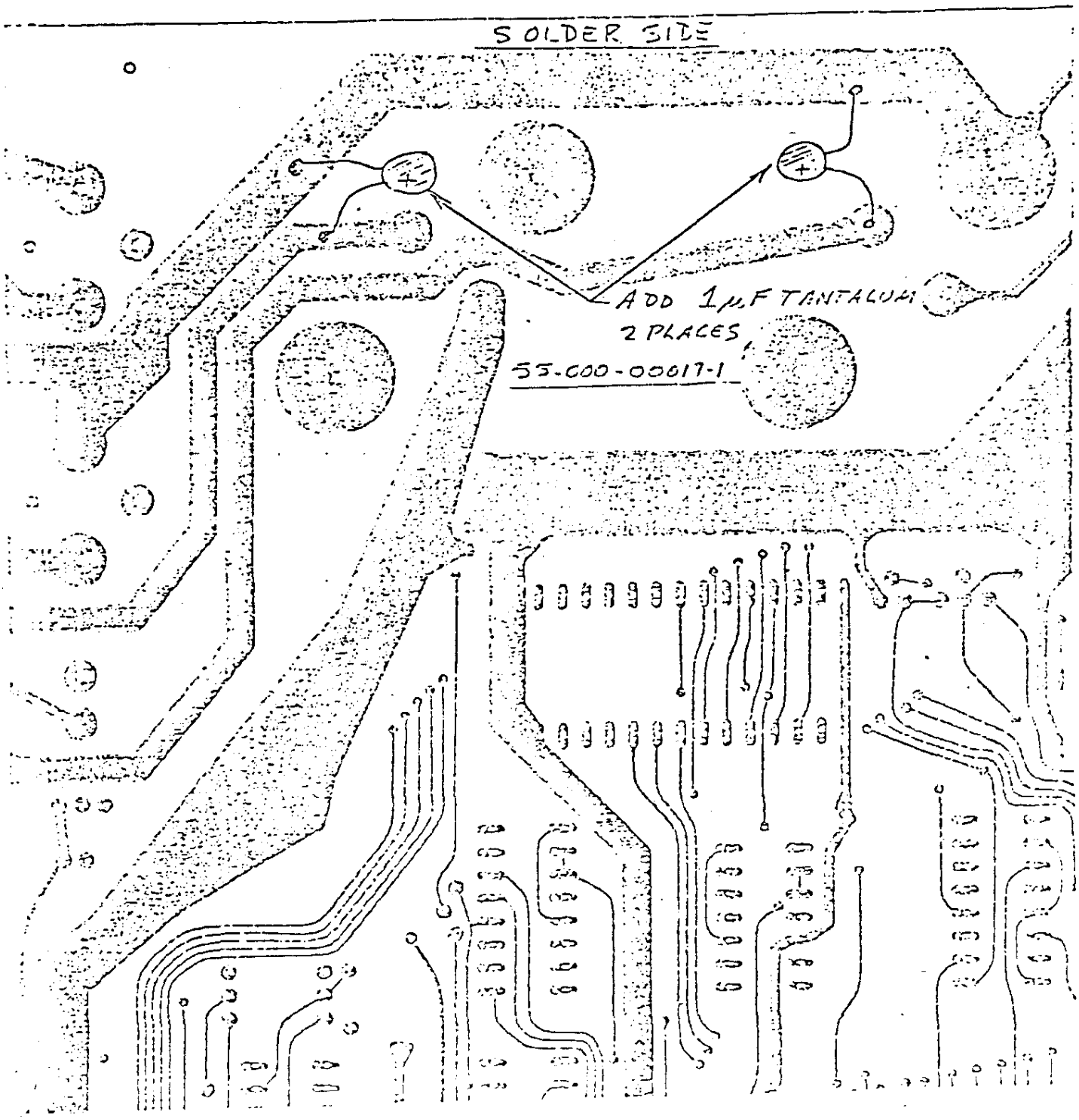


Fig. 1.

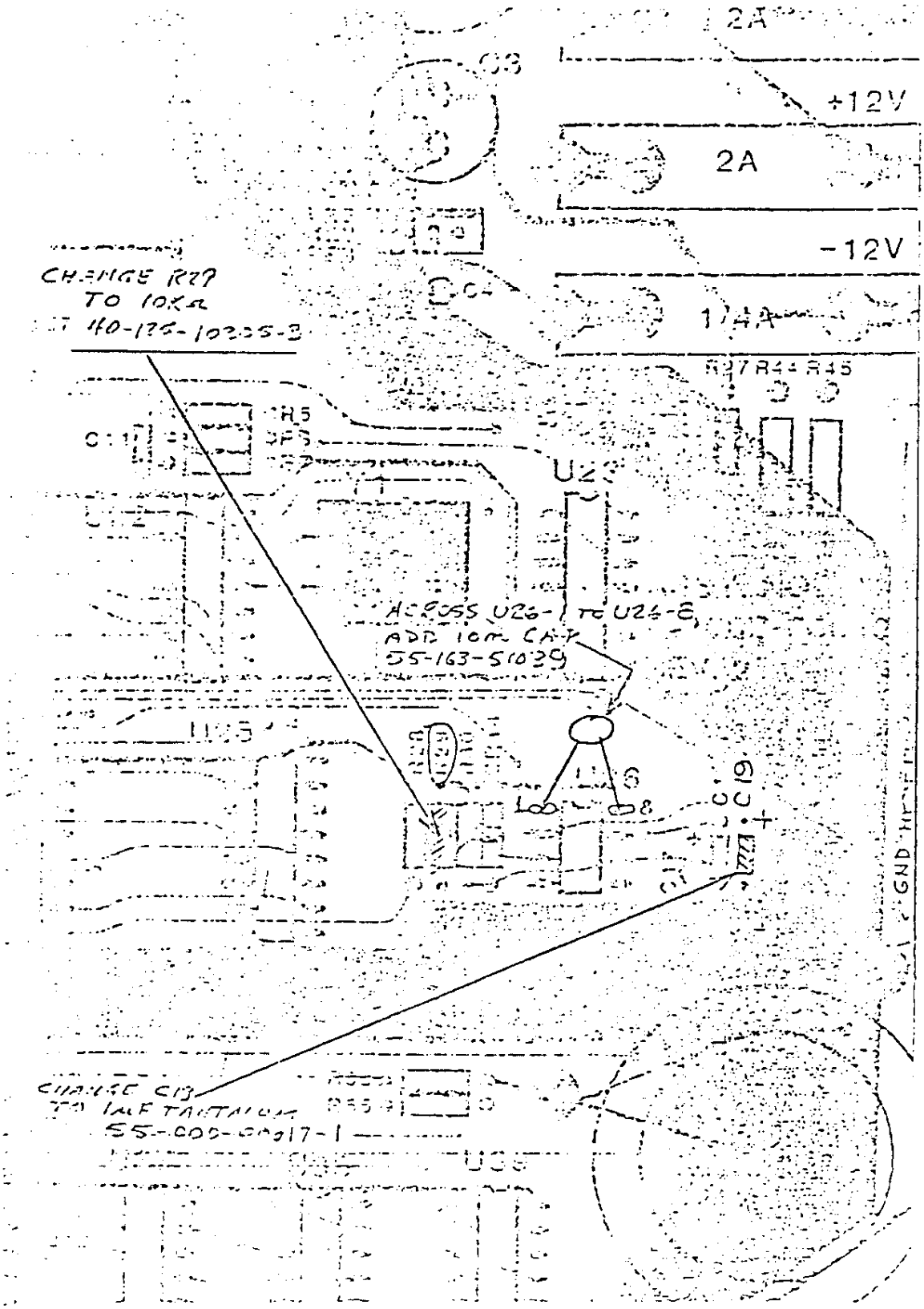

2A
+12V
2A
-12V
1/4A
CHANGE R27
TO 10KΩ
R27 R44 R45
U26
ACROSS U26-1 TO U26-8
ADD 10MFD CAP
55-163-51039
C19
GND
CHANGE C13
TO 1MFD TANTALUM
U26

Fig. 2.

1.0 CONTENTS

This manual may be used for repairing the Volker-Craig VC4404 terminal. It contains circuit descriptions, block diagrams and schematics for the various boards and assemblies contained in the terminal. Any comments and suggestions on this manual are welcome. Please address them to:

Volker-Craig Ltd.
338 Weber Street N.
Waterloo, Ontario
Canada, N2J 3H6

Volker-Craig reserves the right to make improvements to products without incurring any obligation to incorporate such improvements in units previously sold. Specifications and information herein are subject to change without notice.

2.0 SERIAL NUMBERS

All products and components (ie. terminals, circuit boards, etc.) contain model and/or part numbers and a unique serial number. This allows the company to keep records for service purposes. For each terminal shipped, the plant maintains a record which shows the level of upgrading associated with that terminal. Service documentation is also kept for each terminal. The terminal serial number must be referenced when corresponding with the company regarding service or any other reason concerning a particular terminal.

3.0 NON-DISCLOSURE

The VC4404 video data terminal is built in a modular fashion to provide flexibility in options, upgrading and servicing. The unit consists of the power supply, logic and display monitor in one enclosure and the keyboard in a separate enclosure.

All components in the main enclosure may be accessed by removing two screws at the lower rear part of the top cover. The cover is then easily lifted off.

The logic and power supply are located on the main board which is mounted on the bottom of the chassis. The monitor board is mounted on the bezel support bracket at the side of the enclosure.

The keyboard has its own enclosure and is connected to the main logic via a coiled cord which is terminated at both ends with a modular phone jack. The cord may be disconnected at the main enclosure end easily with no tools required. The cover of the keyboard must be removed to disconnect the keyboard end of the cable.

1.0 INTRODUCTION

The keyboard part number 70-250-00007-3 is used on the VC2XXX, VC3XXX and VC4XXX series terminals. The keyboard is microprocessor controlled. It has an auto-repeat function and its output is either two or three bytes of serial data. To remove the keyboard from the enclosure, remove the two screws from the rear of the top cover, remove the top cover and remove the screws from the keyboard.

2.0 FUNCTIONAL DESCRIPTION

2.1 MICROPROCESSOR

The heart of the keyboard is the microprocessor, IC number U5. Three models of microprocessor can be used: the 8048 with 1024 bytes of on-board ROM and 64 bytes of on-board RAM; the 8748 with 1024 bytes of on-board EPROM and 64 bytes of on-board RAM; the 8035 with 64 bytes of on-board RAM but no on-board ROM. When using the 8035, external ROM or EPROM must be installed in position U8 and IC no. U7 must also be installed. These two parts are not installed if using the 8049 or 8748 microprocessor. IC no. U7 is an 8 bit latch which must store the current memory address because the 8035 uses the data bus for both addressing and data transfer.

The functions performed by the microprocessor are set by the program stored in the ROM OR EPROM. The clock rate of the microprocessor is 6 MHz which is set by crystal, Y1.

2.2 KEY MATRIX SCANNING

The microprocessor outputs a binary count on its port, P20 to P23. (It also uses this port to do part of the addressing to the external ROM/EPROM.) Diagnosing this port would be difficult because the output does not count at an even frequency and there is also other data appearing on this bus. The count from the output port goes to two decoder chips, U2 and U3. At each count, one output from the decoder goes low starting at U2-9 and moving across the decoder outputs on consecutive pins. A complete matrix scan occurs once every 30 milliseconds.

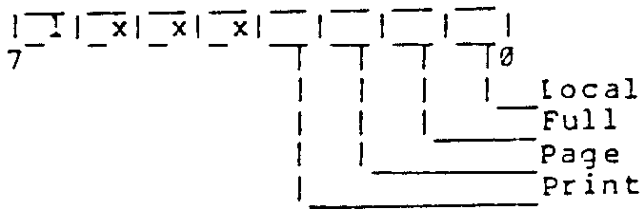
If a key is depressed (contacts shorted), the output from the decoder is shorted to the appropriate input port address of the microprocessor, P11 to P17. After each binary count from its output port, the microprocessor reads its input port and if one of the input addresses is low, the microprocessor knows the matrix address from the combination of the output count and the input address that is low. To diagnose the outputs from the decoders, a key on each decoder output must be depressed because the pull-up resistors are on the opposite side of the keys from the decoders.

2.3 KEYBOARD OUTPUT

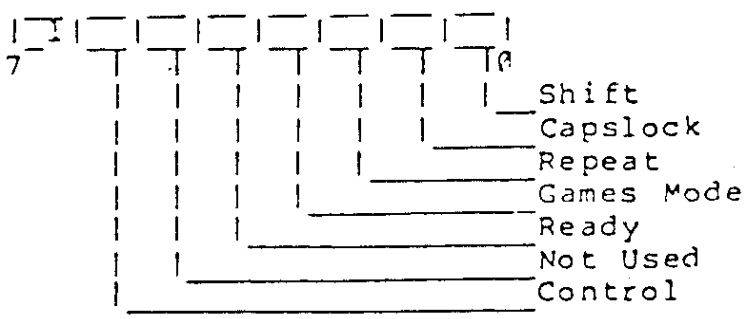
If a key closure is detected, a two or three byte transmission of serial data will occur. These bytes will be status and data as shown below. If the key has been debounced the games mode bit will be reset. If the key has remained down long enough for repeating, the repeat bit will be set. Otherwise the key will be reported with the games mode bit set if this feature has been strap selected.

On the VC4XXX, an additional transmission will occur when the position of any of the following keys are changed: Print, Page, Full, local, Control, Caps lock, or Shift. The data byte will be set to 07FH. These keys are isolated from the input port of the microprocessor by diodes because the Print, Page, Full, local and Caps lock keys are alternate action keys and when they are closed, without the diodes installed, they could cause fantom characters when another key on the same matrix line is pressed.

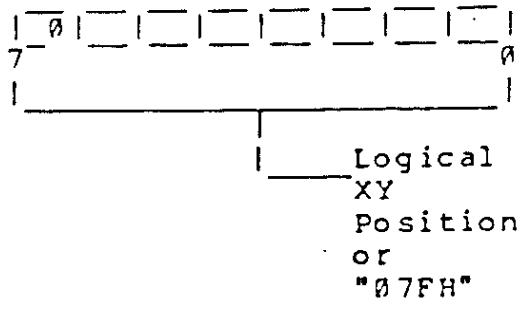
Status 0 (VC4XXX Only)



Status 1



Data



2.4 POWER

The keyboard uses a four wire coiled cable with a modular jack on each end for data transfer to the controller and for power. One wire is used for data, two wires are used for ground and one wire is used for power to the keyboard. The VC3XXX and VC2XXX supply +5 volts to the keyboard. This supply goes directly to the logic on the keyboard. The VC4XXX supplies +8 volts to the keyboard where it is regulated to +5 volts by a 7805 voltage regulator.

2.5 DIAGNOSTICS

An LED is mounted on the keyboard to indicate diagnostic results. It is visible through an opening in the under side of the keyboard housing.

The microprocessor will test RAM read/write and ROM checksum automatically on power up. The diagnostic LED will flash 4 times during ROM check and twice during RAM check. Flashing will be on approximately one half second intervals.

3.0 JUMPERS

Drawing 00-250-00112 sheet 2 shows which jumpers should be installed for each model of terminal.

VC4404 HARDWARE DESCRIPTION.

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11 March 1982 VC4404 TM-01

The VC4404 terminal has had many revisions to improve reliability and operation. This document describes the revisions and their purpose. Any documentation (schematics, board layouts, etc.) should be changed to reflect the revisions. Any VC4404 terminals with a serial number of 23044-XXX or higher will be equipped with all of these revisions. Terminals with lower serial numbers may have part of the revisions or none of the revisions. Whether the revisions should be installed on all of a customer's VC4404 terminals is the customer's decision. A description of the revisions follows.

A. The monitor board, MON-4, had a tendency to give poor focus. The solution to this problem is to improve the frequency response of the video circuit, Change Q10 from a MPS8099 to a 2N2102, change C13 from n47 to n22 and change R36 from 2K2 ohms to 910 ohms.

B. The monitor board would sometimes send a large voltage spike back through the vertical drive signal and destroy the vertical driver on the logic board. The solution is to ground the aquadag of the tube (black area on bell of tube) better. There is a wire braid covered with sleeving attached to one of the bolts on the CRT. If the other end of the braid is attached to the logic board, remove it from the logic board and attach it to the monitor board at the horizontal ground at connector pin 5. Also fasten a piece of copper braid across the tube with a ring fastener to a CRT bolt and a coil spring and ring fastener to the CRT bolt diagonal to the first one. The spring is used to keep tension on the braid. If the monitor is a MON-4, install a 5.2V zener diode (IN5232B) from edge connector pin 9.

C. The video drive transistor on the Sam Sung monitor did not have a high enough voltage rating. Change C201 from a 150pF to 470pF and change Q201 from a 2N2219A to a BF257, BF258, BF259 or 2N2102. If using a 2N2102, also change R202 from 470 ohms to 3K3 ohms and change R203 from 47 ohms to 68 ohms.

D. The Sam Sung monitor had a problem where the display lines could not be made wide enough. To solve this problem, install a 0.01 uF, 400V capacitor in parallel with C409.

.../2

E. Noise was getting into the horizontal drive signal on the logic board and U26 was susceptible to noise and static shock which would cause reset signals at random times. Install a luF tantalum capacitor from the input of VR1 to ground and from the input of VR2 to ground. See fig.1. Change R29 from 1M ohm to 10K ohms, change C19 from .01uF to a luF tantulum and install a 10n capacitor from U26 pin 1 to U26 pin 8. See fig. 2. Shorten the logic board to 16 cm, install an 18 GA jumper from the chassis ground connection to the ground end of R45 and remove J11. Shorten the green/yellow wire from the power connector filter on the rear of the chassis to 10 cm.

1 = JUMPER IN
0 = JUMPER OUT
BLANK = DON'T CARE

REVISION				
REV	DESCRIPTION	DWN	DATE	CHK
2	ADDED SHT. 2/EC00155	DCB	2 JUL 1990	
3	ADDED Δ NOTE J11-GRP 3+4 WAS 0 J27 ALL GRPS WERE BLANK J31 ALL GRPS WERE BLANK EC00264	DCB	21 NOV 90	DC

	CONFIGURATION	PRODUCT	JUMPERS																													Δ
			J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20	J21	J22	J23	J24	J25	J26	J27	J28	J29	J30	J31
GROUPS	GROUP 1	404 NARROW	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0					0		0	0			1
	GROUP 2	404 WIDE	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0					0		0	0			1
	GROUP 3	41X NARROW	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0					0		0	1			0
	GROUP 4	41X WIDE	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0					0		0	1			0
	GROUP 5	VC2XXX	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1					1		0	0			0
	GROUP 6																																
CHARACTER SETS	AZERTY	VC404																					1	0	0	0							
	NORWEGIAN	VC404																					0	1	0	0							
	SWEDISH	VC404																					1	1	0	0							
	DANISH	VC404																					0	1	0	0							
	CSA FRENCH	VC404																					0	0	0	0							
	STANDARD(USA)	VC404																					0	0	0	0							
REMOTE	INTERNAL	ALL																													1	0	
	EXTERNAL	ALL																													0	1	
BOOT MODE	ENABLED	VC2500 ONLY																										1					
	DISABLED	ALL OTHERS																										0					

Δ - J31 IS A FLYWIRE

volker·craig limited
WATERLOO ONTARIO

DCB

PROJECT

SCHEMATIC SERIAL KEYBOARD

SECTION 1

VC4404 CONTROLLER BOARD OPERATIONAL OVERVIEW

THE 4404 CONTROLLER BOARD USES STATE-OF-THE-ART LSI, ALONG WITH A SOPHISTICATED HARDWARE/SOFTWARE ARCHITECTURE TO GREATLY REDUCE THE BOARD AREA NEEDED TO IMPLEMENT THE CRT TERMINAL FUNCTIONS. A FLEXIBLE CPU SYSTEM TIES TOGETHER VIDEO, CONTROL, AND COMMUNICATIONS DATA INTO A COMPACT SOFTWARE DRIVEN STRUCTURE REDUCING CONTROLLER COST, AND BOARD AREA.

THE 4404 HARDWARE STRUCTURE IS BUILT AROUND A "TIME DOMAIN MULTIPLEXED" DATA AND ADDRESS BUS, WITH A MICROPROCESSOR AND A VIDEO CONTROL PROCESSOR RUNNING INTERLEAVED. ~~THE MAIN PROCESSOR CONTROLS~~ INFORMATION FLOW BETWEEN THE TWO COMMUNICATIONS PORTS, THE KEYBOARD, AND THE VIDEO RAM. THIS PROCESSOR ARRANGES INFORMATION TO BE DISPLAYED IN THE VIDEO RAM FOR CORRECT PRESENTATION. THE "VIDEO CONTROL PROCESSOR" HAS TWO MAIN FUNCTIONS: 1) IT GENERATES THE ADDRESS TO ACCESS THE PROPER LOCATIONS IN VIDEO RAM; AND 2) IT GENERATES THE HORIZONTAL, AND VERTICAL "SYNC" SIGNALS FOR PROPER SYNCHRONIZATION OF THE VIDEO DISPLAY.

SECTION 2

THE MICROPROCESSOR SUB-SYSTEM

SECTION 2.1 PROCESSOR UTILIZATION OVERVIEW

THE VC4404 CONTROLLER BOARD USES A FAIRLY STANDARD MICROPROCESSOR STRUCTURE INVOLVING CPU, RAM, ROM, AND I/O. THIS BOARD, HOWEVER, MAKES USE OF THE FACT THAT THE MAIN PROCESSOR (SY 6502) DOES NOT ACTIVELY "USE" THE DATA BUS DURING A CERTAIN PORTION OF IT'S CLOCK CYCLE. DURING THIS "DEAD" TIME, THE VIDEO CONTROL PROCESSOR IS GENERATING THE REQUIRED SIGNALS USING SOME OF THE SAME STRUCTURE WHICH THE MAIN PROCESSOR USES. SUCH MULTIPLEXING MEANS THAT DATA, AND TO SOME EXTENT ADDRESS INFORMATION IS CONSTANTLY CHANGING, AND IS NOT EASY TO TRACK WHEN DE-BUGGING. ALSO, ONE OF THE TWO PROCESSOR SYSTEMS MAY NOT WORK, WHILE THE OTHER ONE FUNCTIONS CORRECTLY. IT IS ALSO OF INTEREST TO NOTE THAT FOR EACH VIDEO ACCESS CYCLE, WHICH IS THE SAME TIME DURATION AS A MAIN PROCESSOR CLOCK CYCLE, TWO CHARACTERS IN VIDEO RAM ARE ACCESSED, TWO ASCII BYTES ARE INPUT INTO THE CHARACTAR ROM, AND TWO 8 BIT BYTES OF SERIAL DATA ARE LATCHED IN PARALLEL INTO TWO 8 BIT SHIFT REGISTERS. THIS ALLOWS THE MAIN CPU TO RUN AT 1/2 THE ACTUAL CHARACTER RATE.

SECTION 2.2 THE MAIN PROCESSOR, U19

THE MAIN PROCESSOR ON THE VC 4404 CONTROL BOARD IS AN SY6502, WHICH IS AN 8 BIT MICROPROCESSOR WITH A 65K ADDRESS SPACE, AND AN INTERNAL CLOCK GENERATOR. THE ADDRESS BUS OF THIS DEVICE IS CONNECTED TO THE VIDEO RAM MULTIPLEXER, THE UARTS, THE SWITCH CIRCUITRY, AND THE CONTROL ROM. THE DATA LINES OF THIS PROCESSOR CONNECT TO THE ON-BOARD DATA BUS WHICH IS SHARED WITH THE REST OF THE PROCESSOR STRUCTURE. U26, A TIMER IC, RESETS THIS CPU, WHICH ALSO FIELDS ALL "IRQ"'S. THE "PHASE TWO" CLOCK OF THIS DEVICE IS ALSO USED TO CONTROL THE SWITCHING OF THE VIDEO RAM ADDRESS MULTIPLEXERS.

SECTION 2.3 THE VIDEO CONTROL PROCESSOR, U20

THIS SPECIAL PROCESSOR SHARES THE DATA BUS WITH THE MAIN PROCESSOR, AND IS ALSO RESET BY U26. IT ALSO HAS AN INTERNAL CLOCK GENERATOR WHICH IS DRIVEN 180 DEGREES OUT OF PHASE WITH THE MAIN CPU'S CLOCK, TO ACCOMPLISH THE TIME DOMAIN SHARING OF THE PROCESSOR STRUCTURE. SOME OF IT'S OUTPUT LINES ARE USED TO GENERATE VIDEO SYNC SIGNALS, AND OTHERS ARE USED TO GENERATE VIDEO RAM ADDRESSES USED TO ACCESS THE PROPER CHARACTER IN VIDEO RAM CORRESPONDING TO WHERE THE MONITOR IS SCANNING.

SECTION 2.4 THE ADDRESS MULTIPLEXERS, U12-16

EACH OF THESE DEVICES IS A QUAD, TWO-TO-ONE MULTIPLEXER (74LS157), AND TOGETHER THEY ARE RESPONSIBLE FOR GATING THE RIGHT ADDRESS BUS (MAIN OR VIDEO) ON TO THE VIDEO RAM ADDRESS BUS AT THE RIGHT TIME. AS SAID BEFORE, THE "SELECT" LINES OF THESE DEVICES ARE DRIVEN BY "PHASE TWO" OF THE MAIN PROCESSOR.

SECTION 2.5 THE LOWER ORDER VIDEO ADDRESS COUNTER, U17

THIS COUNTER, A 74LS93, GENERATES THE 3 LOWER ORDER ADDRESS LINES FOR THE VIDEO PROCESSOR. THIS COUNTER IS INCREMENTED AT HALF THE CHARACTER CLOCK RATE, AND IT'S OUTPUTS ARE CONNECTED TO THE VIDEO RAM THROUGH THE ADDRESS MULTIPLEXERS. THIS CHIP IS CONNECTED IN THE DIVIDE BY EIGHT MODE, AND SO THE "QA" OUTPUT IS NOT USED.

SECTION 2.6 THE VIDEO RAM, U6-9

THESE RAM CHIPS CONSTITUTE THE ONLY RAM ON THE VC4404 CONTROLLER BOARD, AND SO SERVE A VARIETY OF PURPOSES. THE SCREEN MEMORY IS LOCATED IN THIS RAM, AS IS THE MAIN PROCESSORS STACK. ALONG WITH THIS, THE MAIN PROCESSOR'S CONSTANT STORAGE, AND THE VC4404'S INCOMING CHARACTER BUFFER ARE ALL LOCATED HERE. A FEW BYTES OF THIS RAM ARE USED FOR SOME INTERFACING BETWEEN THE MAIN CPU, AND THE VIDEO CONTROL PROCESSOR.

THE ADDRESS, CHIP SELECT, AND READ/WRITE LINES FOR THE RAM COME FROM THE ADDRESS MULTIPLEXERS, AND THE DATA OUTPUTS OF THESE RAMS ARE CONNECTED TO THE INPUTS OF THE CHARACTER ROMS. THESE DATA LINES ARE ALSO COUPLED TO THE ON-BOARD DATA BUS, AND SO, TO THE REST OF THE DATA LINES OF THE CPU STRUCTURE, THROUGH 1K OHM RESISTORS (RP1, AND RP2) TO ALLOW VIDEO INFORMATION TO PROCEED TO THE VIDEO RAM WHILE THE MAIN PROCESSOR IS USING THE REST OF THE CPU STRUCTURE'S DATA BUS.

SECTION 2.7 CHARACTER ROMS, U2,U5

THESE ROMS ARE RESPONSIBLE FOR TRANSLATING TWO INFORMATION INPUTS INTO ONE 8 BIT BYTE WHICH IS THEN SHIFTED OUT SERIALLY AS VIDEO INFORMATION. THESE OUTPUTS ARE LOADED INTO TWO 8 BIT SHIFT REGISTERS, U3, AND U4. THE TWO INFORMATION INPUTS ARE: 1) ASCII INFORMATION OUT OF VIDEO RAM, AND 2) RASTER INFORMATION FROM THE RASTER COUNTER, U1. (SEE SECTION 2.9.) THESE TWO "BUSSES" OF INFORMATION ARE VALID UNTIL AN ACTUAL "SET" (16 BITS) OF SERIAL DATA HAS BEEN LATCHED INTO THE VIDEO SHIFT REGISTERS, U3, AND U4.

SECTION 2.8 PARALLEL TO SERIAL CONVERSION, U3,U4

TWO SHIFT REGISTERS, (BOTH ARE 74LS165'S) ARE USED TO TRANSFORM 16 BITS (TWO CHARACTERS WORTH) OF PARALLEL DATA FROM THE CHARACTER ROMS, INTO VIDEO DATA. THIS DATA IS "HI" OR "LO", TO TURN THE ELECTRON GUN OF THE CRT MONITOR "ON" OR "OFF" AS SHIPPED FROM THE FACTORY. THE 8 INPUTS TO EACH OF THESE SHIFT REGISTERS ARE GENERATED BY THE DATA OUTPUTS OF THE CHARACTER ROMS. THESE OUTPUTS ARE LATCHED INTO THE SHIFT REGISTER INPUTS, WHEN VALID, BY A LOAD CLOCK (GENERATED BY THE CLOCK CIRCUITRY, SECTION 6.4) WHICH CONNECTS TO PIN 15, (SHIFT/LOAD) OF THE TWO SHIFT REGISTERS. (THIS SAME CLOCK CIRCUITRY ALSO GENERATES THE CHARACTER DOT CLOCK, WHICH CONTROLS THE SHIFTING OUT OF VIDEO "DOTS", SECTION 6.4.)

THE "SHIFT IN" (SI) INPUTS OF THESE CHIPS ARE CONNECTED, THROUGH J3, TO EITHER +5 VOLTS (HI), OR GROUND (LO). THE PURPOSE FOR THIS JUMPER IS TO FILL THE SHIFT REGISTER (AS DATA IS BEING SHIFTED OUT) WITH EITHER ALL "0", OR ALL "1", SO THAT WHEN NO DATA IS BEING LOADED INTO THESE SHIFT REGISTERS (DURING BLANKING FOR EXAMPLE) THESE REGISTERS CONTAIN THE CORRECT DATA TO PRODUCE A "SPACE", OR NO CHARACTER IN EITHER "NORMAL BACKGROUND", OR "REVERSE BACKGROUND" MODE.

SECTION 2.9 THE RASTER COUNTER, U1

THIS 4 BIT COUNTER IS CONNECTED AS A DIVIDE BY TEN COUNTER WHICH IS INCREMENTED ONCE EVERY HORIZONTAL LINE BY THE VIDEO CONTROL PROCESSOR. THE OUTPUTS OF THIS COUNTER ARE CONNECTED TO SOME OF THE ADDRESS INPUTS OF THE TWO CHARACTER ROMS. FUNCTIONALLY, THIS COUNTER ADDRESSES THE CORRECT "RASTER LINE" OR ROW OF THE CHARACTER CURRENTLY BEING SCANNED ACROSS. THE SAME "ROW" OF 80 DIFFERENT CHARACTERS POSITIONS IS SCANNED IN ONE HORIZONTAL LINE, REQUIRING THIS COUNTER TO BE INCREMENTED ONCE FOR EACH LINE.

SECTION 2.10 THE ADDRESS DECODER, U34

THE MAIN PROCESSOR MEMORY MAP (SEE APP. A) REQUIRES THAT CERTAIN SUB-SYSTEMS APPEAR AT CERTAIN ADDRESSES WITHIN THE 6502'S 65K ADDRESS SPACE. THE POSITIONING OF THESE SUB-SYSTEMS IS CONTROLLED BY THE ADDRESS DECODER, U34, A 74LS139. THE SELECT INPUTS OF THIS DEVICE ARE CONNECTED TO THE HIGHEST ORDER ADDRESS LINES, A13-15. THE ACTIVE LOW OUTPUTS OF THIS CHIP ARE USED TO SELECT THE VARIOUS CHIPS WHICH THE MAIN CPU ACCESSES; THE UARTS, THE VIDEO RAM, ETC..

SECTION 2.11 THE PROGRAM ROM, U10,U11

THIS 4K X 8 ROM/EPROM (U11) CONTAINS THE CONTROL PROGRAM WHICH IS EXECUTED BY THE MAIN PROCESSOR TO PERFORM IT'S FUNCTIONS SUCH AS HANDLING COMMUNICATIONS DATA, READING SWITCHES, AND ORDERING DATA IN THE VIDEO RAM FOR DISPLAY. THIS ROM CONTAINS ALL THE REGULAR CONTROL AND POLLING ROUTINES, AS WELL AS AN EXTENSIVE SET OF DIAGNOSTICS FOR THE VARIOUS ON-BOARD SUB-SYSTEMS. THIS ROM ALSO CONTAINS INFORMATION USED BY THE VIDEO CONTROL PROCESSOR TO ACCOMPLISH IT'S FUNCTION. THE ADDRESS LINES OF THIS ROM ARE CONNECTED TO THE SAME MULTIPLEXED ADDRESS BUS WHICH THE VIDEO RAM USES. THE DATA LINES OF THIS ROM ARE CONNECTED TO THE VC4404 VIDEO CONTROLLER'S DATA BUS THROUGH AN OCTAL, TRI-STATE BUFFER, U10 (A 74LS244) TO ENSURE THAT THE DATA FROM THIS ROM IS GATED ON THE DATA BUS AT THE CORRECT TIME.

SECTION 3

VIDEO SECTION

SECTION 3.1 VIDEO OVERVIEW

THE VIDEO OUTPUT STAGE CAN BE BROKEN DOWN INTO TWO SECTIONS; THE "MONITOR" SECTION, AND THE "COMPOSITE" SECTION. THE MONITOR VIDEO OUTPUTS ARE USED TO DRIVE AND SYNCHRONIZE THE MONITOR CRT WHICH IS ACTUALLY MOUNTED INSIDE THE VC4404 CHASSIS. THE COMPOSITE OUTPUT IS USED BY AN EXTERNAL VIDEO DISPLAY DEVICE, AND THEREFORE MUST BE BROUGHT OUTSIDE OF THE VC4404 ENCLOSURE. THERE ARE THREE OUTPUTS WHICH ARE CONNECTED TO THE MONITOR CIRCUITRY, AND THEY ARE "VIDEO", "HORIZONTAL SYNC", AND "VERTICAL SYNC". THE COMPOSITE OUTPUT, ON THE OTHER HAND, COMBINES THESE THREE SIGNALS INTO ONE "COMPOSITE" SIGNAL WHICH CONTAINS VIDEO, HORIZONTAL SYNC, AND VERTICAL SYNC INFORMATION. THE VIDEO OUTPUT SECTION ALSO INCLUDES CIRCUITRY TO PRODUCE "LO INTENSITY", AND ALSO "PULSE STRETCHING" CIRCUITRY TO ACCOMODATE THE NARROW BANDWIDTH OF SOME VIDEO MONITORS.

SECTION 3.2 THE LOW INTENSITY CIRCUITRY, U24,U25

THE MOST SIGNIFICANT BIT OF THE DATA IN THE VC4404'S VIDEO RAM IS USED TO FLAG WHETHER THE CHARACTER IS TO BE NORMAL, OR LOW INTENSITY. WHEN DATA BIT "D7" IS "CLEARED"; I.E. SET TO ZERO, THE CHARACTER WILL BE DISPLAYED IN LOW INTENSITY. SINCE THE VIDEO RAM DATA LINES ARE COUPLED TO THE SYSTEM DATA BUS THROUGH 1K RESISTORS, ANY EXTRA LOADING ON THESE VIDEO RAM CAN CAUSE RAM DATA ERRORS. TO PREVENT THE HIGH/LO INTENSITY SENSING CIRCUITRY FROM LOADING THESE LINES TOO MUCH, A CMOS (VERY HIGH INPUT IMPEDANCE) INVERTER IS USED TO INTERFACE TO THESE DATA LINES. THE PART USED IS AN RCA CA4049. THE POLARITY OUT OF THESE INVERTERS IS WRONG, SO ANOTHER INVERTER OF THE PACKAGE IS NECESSARY TO CORRECT THE POLARITY. ALSO, ONE OF THESE CMOS INVERTERS CAN ONLY DRIVE TWO "TTL" INPUTS, TWO INVERTERS ARE USED FOR EACH CHARACTER (4 INPUTS OF U24 PER CHARACTER.)

THE OUTPUTS OF THESE INVERTERS OF U25 ARE CONNECTED TO THE PARALLEL LOAD INPUTS OF U24, A 74LS166 SHIFT REGISTER. THE SHIFT CLOCK, AND THE LOAD CLOCK ARE GENERATED BY THE CLOCK CIRCUITRY (SEE SECTION 6.4.) THE LOAD CLOCK IS THE SAME USED FOR THE VIDEO DATA SHIFT REGISTERS, AND INITIATES A "LOAD" ONCE EVERY CPU CYCLE (EX. DURING BLANKING) WHICH LOADS TWO CHARACTERS WORTH OF INFORMATION. THE SHIFT CLOCK FOR U24 IS ALSO THE SAME AS U3, AND U4. FOR THE HIGH/LO INTENSITY SHIFT REGISTER, HOWEVER, THE "CI" OR CLOCK INHIBIT INPUT IS CONNECTED TO A CLOCK WHICH IS ONE HALF THE DOT CLOCK RATE.

THE RESULT OF THIS IS THAT THE HIGH/LO INTENSITY SHIFT REGISTER IS ESSENTIALLY CLOCKED ONCE FOR EVERY TWO VIDEO "DOTS", AND SO ONLY ONE SHIFT REGISTER (ONE BIT FOR EACH TWO DOTS) IS NECESSARY. NOTE THAT ONE CHARACTER CAN STILL BE LO INTENSITY, AND THE OTHER HI INTENSITY, SINCE THE TWO "D7" DATA LINES ARE SEPARATE. THE OUTPUT OF THIS SHIFT REGISTER IS A SIGNAL WHICH TRACKS THE VIDEO OF EACH CHARACTER THAT IS LO FOR LO INTENSITY, AND HIGH FOR NORMAL INTENSITY.

SECTION 3.3 THE VIDEO PULSE STRETCHER, U41

IN ORDER TO ACCOMODATE VIDEO MONITORS WITH A RELATIVELY LOW BANDWIDTH, BOTH THE INTENSITY AND THE VIDEO INFORMATION ARE "STRETCHED" (BY ABOUT A HALF A DOT; THIS MAKES RELATIVELY LITTLE DIFFERENCE IN THE INTENSITY SIGNAL, IT JUST LINES IT UP WITH THE VIDEO) ON A DOT BASIS, REDUCING THE REQUIRED BANDWIDTH DUE TO AN INCREASE IN THE DOT RESOLUTION TIME. SINCE THE CHARACTER ROM USED HAS THE EIGHTH COLUMN OF ALL CHARACTERS BLANK, THE VIDEO INFORMATION IS NEVER OVERLAPPED.

THIS STRETCHING IS IMPLEMENTED BY TWO IDENTICAL CIRCUITS, ONE CIRCUIT TO STRETCH THE INTENSITY, AND ONE CIRCUIT TO STRETCH THE VIDEO. THE CIRCUIT IS COMPOSED OF TWO "OR" GATES (U41, A 74LS32) ONE OF WHICH IS USED SIMPLY TO OR TOGETHER BOTH THE ORIGINAL SIGNAL, AND THE DELAYED SIGNAL. AS HINTED AT, THE OTHER GATE IS SIMPLY A DELAY OF ABOUT A HALF A DOT. THIS IS DONE BY CONNECTING THE OUTPUT OF THE DELAY GATE (PINS 3, OR 11) TO THE INPUT OF THE "OR"ING GATE THROUGH A 1K RESISTOR. THIS RESISTANCE, IN SERIES WITH THE INPUT CAPACITANCE OF THE GATE ITSELF, FORM AN RC TIME CONSTANT, AND SO THE DELAY. "TTL" LEVEL THRESHOLDING PREVENTS USING RESISTOR VALUES MUCH GREATER THAN 1K.

SECTION 3.4 THE FINAL DRIVE OUTPUTS, U29

THIS PART, A 74S86 QUAD EXCLUSIVE OR GATE IS USED BOTH AS A BUFFER, (FOR HORIZONTAL, VERTICAL, AND LO INTENSITY DRIVE,) AND A PROGRAMMABLE INVERTER (FOR VIDEO REVERSING.) THE VIDEO AND LO INTENSITY OUTPUTS ARE CONNECTED TO THE VIDEO OUTPUT STAGE, THE VERTICAL OUTPUT IS CONNECTED DIRECTLY TO THE MONITOR'S VERTICAL SYNC CIRCUITRY, AND THE HORIZONTAL OUTPUT CONNECTS TO THE HORIZONTAL SYNC PULSE STRETCHER, U40.

SECTION 3.5 THE HORIZONTAL SYNC PULSE STRETCHER, U40

THE HORIZONTAL SYNC PULSE GENERATED BY THE VIDEO CONTROL PROCESSOR IS ON THE ORDER OF 5 TO 10 MICRO-SECONDS LONG, AND FOR THE VC4404'S MONITOR, THIS IS TOO SHORT. TO LENGTHEN THIS PULSE, A "ONE-SHOT" IS CONNECTED TO THE HORIZONTAL DRIVE WHOSE OUTPUT IS CONNECTED TO THE MONITOR'S HORIZONTAL SYNC INPUT. THIS PULSE IS STRETCHED TO NOMINALLY 27 MICRO-SECONDS BY THIS ONE-SHOT, A 555 TIMER I.C. THE TIME CONSTANT CHOSEN FOR THIS CHIP IS ON THE EDGE OF THE SPEC'ED DURATION FOR THE 555, AND SHOULD NOT BE SHORTENED.

SECTION 3.6 THE MONITOR VIDEO OUTPUT STAGE

THIS TRANSISTOR, Q3, IS THE FINAL DRIVE TRANSISTOR FOR THE VIDEO OUTPUT TO THE MONITOR. WITH AN INPUT OF TWO DIGITAL SIGNALS, THIS CIRCUIT GENERATES THREE LEVELS OF VIDEO OUTPUT. THESE TWO DIGITAL INPUTS ARE VIDEO, (FROM U29-11, ACTIVE HI AS SHIPPED) AND LO INTENSITY (FROM U29-8, ACTIVE LOW.) THE OUTPUT LEVELS ARE; VIDEO OFF, (ABOUT .1V); LO INTENSITY VIDEO, (ABOUT 2V) AND; NORMAL VIDEO (ABOUT 3V). THE OPERATION OF THIS CIRCUIT IS AS FOLLOWS.

SUPPOSE THE "DOT" SCANNED IS NORMAL VIDEO. IN THIS CASE, THE VIDEO SIGNAL (U29-11, OR U4-13) IS HI, OR LOGIC ONE, SO CR15 IS REVERSE BIASED. ALSO, THIS DOT IS NOT LO INTENSITY, SO U29-8 (U24-13) IS HI ALSO, REVERSE BIASING CR16. WITH BOTH OF THESE DIODES REVERSE BIASED, R14 PULLS THE BASE OF Q3 UP TO +5 VOLTS, AND Q3 IS TURNED "ON" ALL THE WAY. WITH Q3 ON, THE VOLTAGE AT THE EMITTER OF Q3, AND SO, THE VIDEO OUTPUT, IS APPROXIMATED BY THE VOLTAGE AT THE CENTER OF THE RESISTOR VOLTAGE DIVIDER R19/R16, SINCE Vce ON IS .1V.

NOW SUPPOSE THE NEXT DOT IS LO INTENSITY. VIDEO IS STILL HI, AND SO CR15 IS STILL BACK BIASED. LO INTENSITY, HOWEVER, IS NOW LO, WHICH MAKES CR16 CONDUCT. IN THIS CASE, THE BASE VOLTAGE OF Q3 IS DETERMINED BY A RESISTOR DIVIDER R14/R18, AND THE EMITTER VOLTAGE, AND SO THE OUTPUT FOLLOWS THIS VOLTAGE BY Vbe.

IF VIDEO GOES LO. THEN CR15 IS NOW FORWARD BIASED, WHICH PULLS THE BASE OF Q3 DOWN, AND Q3 TURNS OFF. THE EMITTER OF Q3 IS THEN ALMOST AT GROUND.

SECTION 3.6.1 THE CONTRAST CONTROL

THE VOLTAGES GIVEN AT THE BEGINNING OF SECTION 3.6 FOR THE THREE LEVELS OF VIDEO OUTPUT WERE PURPOSELY IMPRECISE, BECAUSE THESE VALUES MUST BE ADJUSTABLE TO IMPROVE OR CONTROL "CONTRAST". TO ACCOMPLISH THIS, THE "TOP" (MOST POSITIVE SIDE) OF THE OUTPUT RESISTOR DIVIDER R19/R16 IS CONNECTED TO THE EMITTER OF A TRUE EMITTER FOLLOWER, Q2. THE COLLECTOR OF Q2 IS CONNECTED TO +12 VOLTS, AND THE BASE IS CONTROLLED BY A VARIABLE RESISTOR MOUNTED ON THE FRONT OF THE VC4404. SINCE Q2 IS AN EMITTER, OR VOLTAGE FOLLOWER, THE VOLTAGE AT THE EMITTER OF Q2, AND SO THE POSITIVE END OF THE VIDEO OUTPUT RESISTOR DIVIDER, FOLLOW THE BASE OF Q2 BY Vbe.

SECTION 3.7 THE COMPOSITE VIDEO OUTPUT STAGE

THIS TRANSISTOR, Q1, USES TWO DIODES (CR16, AND CR17) TO COMBINE TWO DIGITAL SIGNALS LIKE THE MONITOR OUTPUT, BUT THIS CIRCUIT IS DIFFEREFNT IN TWO WAYS WHICH WILL BE DISCUSSED.

FIRST OF ALL, THE VIDEO MONITOR CONNECTED EXTERNAL TO THE VC4404 NEEDS A SOURCE OF HOR./VERT. SYNC INFORMATION TO CORRECTLY DISPLAY THE VIDEO. TO ACCOMPLISH THIS, THE VIDEO CONTROL PROCESSOR GENERATES ONE SIGNAL, "V/H" WHICH HAS ALL THIS INFORMATION ON IT. THIS SIGNAL GOES "HI" WHENEVER A SYNC PULSE IS PRESENT. THIS SIGNAL IS CONNECTED TO A TRANSISTOR, Q5, WHOSE EMITTER IS GROUNDED, AND WHOSE COLLECTOR IS CONNECTED TO THE BASE OF THE COMPOSITE OUTPUT TRANSISTOR, Q1. WHEN SYNC IS "HI", Q5 PULLS THE BASE OF Q1 TO GROUND AND THE COMPOSITE VIDEO SIGNAL GOES LO.

ALSO NOTE THAT THE COLLECTOR OF Q1 IS TIED DIRECTLY TO +5V, SO THAT Q1 IS ALSO A TRUE EMITTER FOLLOWER. BECAUSE OF THIS, ALL OF THE VOLTAGE DIVISION TO ESTABLISH THE CORRECT VIDEO LEVELS (1.4 V FOR NORMAL VIDEO, 1.0V FOR LO INTENSITY, AND .1V FOR VIDEO OFF) MUST BE DONE AT THE BASE OF Q1.

SECTION 4

RS-232-C CIRCUITRY

SECTION 4.1 MAIN/AUXILIARY PORT OVERVIEW

THE VC4404 USES TWO SY6551A UARTS FOR THE TWO REQUIRED SERIAL COMMUNICATION PORTS. THESE TWO PORTS (MAIN AND AUX) ARE SPLIT BETWEEN THE TWO UARTS SUCH THAT THE MAIN PORT CAN TRANSMIT AND RECIEVE AT DIFFERENT BAUD RATES. (THE AUX PORT MUST, OF COURSE, TRACK THESE BAUD RATES.) ALL DATA AND HANDSHAKE LINES FOR BOTH LINES ARE FULLY BUFFERED, AND +/-12 VOLT DRIVEN FOR FULL RS-232-C COMPATIBILITY.

SECTION 4.2 THE MAIN RECIEVE/AUXILIARY TRANSMIT UART, U31

THIS UART PERFORMS RECIEVE HANDSHAKING, AND DATA COLLECTION FOR THE MAIN PORT, AS WELL AS DATA TRANSMISSION FOR THE AUX, OR PERIPHERAL PORT. THE 6551 HAS A FAIRLY STANDARD MICROPROCESSOR INTERFACE, WITH ACCESSES TO IT'S 4 INTERNAL REGISTERS CONTROLLED BY ADDRESS, DATA, R/W, AND CLOCK SIGNALS. THE CHIP SELECT FOR THIS UART IS GENERATED BY THE ADDRESS DECODER, U34. THIS UART'S "IRQ" LINE IS CONNECTED TO THE MAIN PROCESSOR, AS IS THE UART'S RESET LINE. ~~THE 6551 HAS A PROGRAMMABLE BAUD RATE GENERATOR INTERNALLY, WHICH ONLY NEEDS A SOURCE CLOCK. THIS CLOCK, "UCLK" IS GENERATED BY THE CLOCKING~~ CIRCUITRY, SECTION 6.4.

SECTION 4.3 THE MAIN TRANSMIT/AUXILIARY RECIEVE UART, U32

THIS UART HANDLES TRANSMIT DATA, AND HANDSHAKING FOR THE MAIN PORT, AS WELL AS RECIEVE DATA AND HANDSHAKING FOR THE PERIPHERAL PORT. THIS UART INTERFACES TO THE MAIN PROCESSOR SIMILARLY TO U31.

SECTION 4.4 THE RS-232-C BUFFERS, U27,U28,U30,U35

THERE ARE TWO TYPES OF BUFFERS REPRESENTED HERE; ONE TYPE FOR DATA TRANSMISSION, AND ONE TYPE FOR DATA RECEPTION. THE TRANSMITTERS ARE "1488" +/- VOLTAGE DRIVERS WHOSE SUPPLIES ARE CONNECTED TO +12V, AND -12V. THIS VOLTAGE SWING REDUCES NOISE PROBLEMS ASSOCIATED WITH USING A "GROUND" LEVEL AS ONE STATE. THE RECIEVERS ARE THE COMPLEMENTARY PART TO THE 1488, AND ONLY REQUIRE ONE SUPPLY. THESE PARTS ARE "1489" IC'S, AND ARE USED TO BUFFER ALL INCOMING RS-232 SIGNALS. THESE RECIEVERS ARE U30, AND U35.

SECTION 5

POWER SUPPLY

SECTION 5.0 POWER SUPPLY OVERVIEW

THE THREE SUPPLY VOLTAGES WHICH THE VC4404 USES ARE POWERED BY A TRANSFORMER WHOSE PRIMARY IS CONNECTED TO THE AC LINE VOLTAGE THROUGH A LINE FILTER WHICH IS PART OF THE POWER CORD RECEPTACLE. THE TERMINAL WILL OPERATE ON A 110/120 VOLT OR 220/240 VOLT SUPPLY DEPENDING ON HOW A JUMPER BLOCK CONNECTED TO THE PRIMARY OF THE TRANSFORMER IS CONNECTED. THE THREE SECONDARIES USED ARE CONNECTED TO THE VC4404 CONTROL PCB THROUGH THE CONNECTOR MARKED 'POWER'.

THERE IS A FUSE AT THE INPUT OF THE REGULATOR OF EACH OF THE SUPPLIES. THE CIRCUIT BOARD HAS A VOLTAGE MARKED AT EACH FUSE POSITION. THIS VOLTAGE IS THE VOLTAGE OUTPUT OF THE REGULATOR. THE ACTUAL VOLTAGE AT THE FUSE IS MUCH HIGHER.

SECTION 5.1 THE +5 VOLT POWER SUPPLY, VR1

THE SECONDARY USED FOR THIS SUPPLY IS RECTIFIED USING A FULL WAVE BRIDGE RECTIFIER (CR1-4) AND THEN FILTERED (C1) AND THEN REGULATED DOWN TO +5 VOLTS BY VR1, A 7805. THERE IS ALSO A 2A FUSE IN SERIES WITH THE REGULATOR INPUT TO PROTECT THE BRIDGE AND TRANSFORMER IF THE REGULATOR IS OVERLOADED. THE VOLTAGE AT THE FUSE IS APPROXIMATELY +9.5 VOLTS. THE REGULATOR HAS A 'TO-3' CASE WHICH IS MOUNTED ON A HEAT SINK TO DISSIPATE THE HEAT GENERATED IN THE REGULATION PROCESS.

SECTION 5.2 +12 VOLT POWER SUPPLY, VR2

THIS SUPPLY IS ALMOST IDENTICAL TO THE +5 VOLT SUPPLY, EXCEPT THAT A DIFFERENT SECONDARY IS USED, THE BRIDGE IS MADE UP OF CRS-8, THE FILTER IS C2, AND THE REGULATOR, A 7812, IS A +12 VOLT REGULATOR. THE VOLTAGE AT THE 2A FUSE IS APPROXIMATELY +18.5 VOLTS.

SECTION 5.3 -12 VOLT POWER SUPPLY, VR3

THE LOAD ON THE -12 VOLTS IS CONSIDERABLY LESS THAN THE OTHER TWO SUPPLIES, SO THAT THE CASE OF THE REGULATOR IS A "TO-220" TYPE, AND IT IS LEFT FREE-STANDING. THIS REGULATOR IS VR3, A 7912. AGAIN, A DIFERENT SECONDARY IS USED FOR THIS SUPPLY, AND IT'S OUTPUT IS RECTIFIED BY CR9, A SINGLE HALF-WAVE RECTIFIER. C3 IS THE FILTER FOR THIS SUPPLY, AND IT IS PROTECTED BY A 1/4A FUSE. THE VOLTAGE AT THE FUSE IS APPROXIMATELY +9.5 VOLTS.

SECTION 6

MISCELLANEOUS CIRCUITRY

SECTION 6.1 THE OPTION SWITCH CIRCUITRY, U36-39

THIS CIRCUITRY IS USED TO READ THE VC4404'S 16 OPTION SWITCHES. THESE SWITCHES, ARE MADE UP OF TWO 8 POSITION "PIANO" DIP SWITCHES, WHICH ARE ACCESSABLE THROUGH THE BACK OF THE VC4404. THESE 16 SWITCHES ARE SET UP IN A 4 BY 4 MATRIX. THE COLUMN DRIVERS ARE 74LS05 OPEN COLLECTOR INVERTERS, WHOSE OUTPUTS GO "LO" IN RESPONSE TO A "HI" ON MAIN PROCESSOR ADDRESS LINES A0-A3. WHEN READING, THESE LINES ARE "RAISED" ONE AT A TIME (ONE COLUMN AT A TIME) FORCING ANY ROW WITH A SWITCH (OF THE SELECTED COLUMN) CLOSED, TO GO LOW.

EACH ROW IS "PULLED-UP" TO +5 VOLTS BY RESISTORS R40-R43. ALSO, THESE ROWS ARE CONNECTED TO THE INPUTS OF 4 OF THE SIX BUS DRIVERS IN U36, A 74LS368 HEX BUS DRIVER, WHICH INTERFACES WITH THE BOARD'S DATA BUS WHEN SELECTED BY THE ADDRESS DECODING, U34. (50/60 HZ, AND J12 IS ALSO READ THROUGH THIS BUFFER.) WHEN ONE COLUMN OF SWITCHES IS SCANNED, READING THIS BUFFER TELLS WHICH SWITCHES ARE CLOSED.

SECTION 6.2 THE RESET TIMER, 26

THIS DEVICE, A 555 TIMER IC IS USED TO RESET BOTH THE MAIN AND VIDEO PROCESSOR, AND ALSO ALL THE LSI PERIPHERAL CHIPS ON THE VC4404. THIS TIMER IS SET UP IN THE "ONE-SHOT" MODE, WITH A PULSE DURATION OF ABOUT 50 MILLISECONDS. THIS ONE-SHOT MAY ALSO BE TRIGGERED BY SHORTING TO GROUND THE PAD ON THE VC4404 CONTROL BOARD MARKED "RESET".

SECTION 6.3 THE BELL CIRCUIT, U28,U33,U39

THE BELL USED ON THE VC4404 IS A PIEZOELECTRIC SPEAKER. IT IS DRIVEN BY A SPARE RS-232 DRIVER, PINS 11-13 OF U28, A 1488, TO ALLOW A FULL +/- VOLTAGE SWING TO INCREASE THE OUTPUT AMPLITUDE OVER USING JUST +5 VOLTS. THE KEYBOARD UART'S TRANSMIT LINE IS USED TO ENABLE THE BELL. WHEN THE SOFTWARE WISHES TO ACTIVATE THE BELL, THE UART (U33) IS PLACED IN THE BREAK MODE, CAUSING THE "TXD" OUTPUT TO GO LO FOR THE LENGTH OF THE BREAK. THIS LO IS INVERTED BY U39, AN OPEN COLLECTOR INVERTER, AND IT'S PULL-UP, R39.

THE FREQUENCY OF THE BELL IS ACTUALLY DETERMINED BY THE SIGNAL AT PIN 13 OF U28 (MARKED "BELL"). THIS SIGNAL IS CONNECTED TO RASTER ADDRESS LINE A1, SINCE IT IS CONTINUALLY COUNTING. THIS MAKES THE BELL FREQUENCY ABOUT 4 KHZ.

SECTION 6.4 THE CLOCK CIRCUITRY, U18,U21-23

THIS CIRCUITRY GENERATES THE NECESSARY CLOCKS TO ALLOW THE VC4404 TO FUNCTION PROPERLY. ALL OF THE CLOCKS GENERATED ARE DERIVED FROM A 14.745 CRYSTAL OSCILLATOR. A DIVIDER, U23, DIVIDES DOWN THIS MAIN CLOCK INTO LOWER FREQUENCY CLOCKS. SOME OF THESE CLOCKS ARE USED DIRECTLY, AS THE CASE OF "UCLK" WHICH IS CONNECTED TO THE "QC" OUTPUT OF U23, THE DIVIDE BY 8 OUTPUT. OTHERS, LIKE THE LOAD-CLOCK (U3,U4, AND U24 PIN 15) ARE GENERATED BY ACTUALLY GATING TOGETHER AND INVERTING MANY CLOCKS. THESE CLOCKS ARE TYPICALLY QUITE COMPLICATED. THE MAIN AND VIDEO PROCESSOR'S CLOCKS ARE GENERATED USING A J-K FLIP-FLOP, (U18) WHICH AMONG OTHER THINGS SUPPLIES TWO CLOCKS WHICH ARE IN TIME SYNCHRONIZATION, BUT EXACTLY OPPOSITE IN POLARITY.

SECTION 6.5 THE KEYBOARD UART, U33

THIS UART INTERFACES TO THE VC4404'S CPU STRUCTURE LIKE THE OTHER TWO UARTS. IT'S TRANSMIT SECTION CONTROLS THE BELL (SECTION 6.3) BUT IT'S RECIEVE SECTION IS USED TO RECIEVE INFORMATION FROM THE VC4404'S KEYBOARD. THIS KEYBOARD CONNECTS TO THE VC4404 CONTROL BOARD AT THE CONNECTOR MARKED "KEYBOARD", FROM WHICH THE KEYBOARD ALSO DERIVES IT'S POWER. THE KEYBOARD'S DATA LINE IS DECOUPLED, AND CLAMPED BEFORE ENTERING THE UART.

APPENDIX A

MEMORY MAP

SUB-SYSTEM	ADDRESS
	FFFF
CONTROL ROM	
	F000
********** (NOT USED) **********	
	B800
SWITCHES, 50/60 HZ, JUMPER J12	
	B000
********** (NOT USED) **********	
	7804
U32 MAIN PORT TRANSMIT UART	
	7800
********** (NOT USED) **********	
	5804
U31 MAIN PORT RECEIVE UART	
	5800
********** (NOT USED) **********	
	3804
U33 KEYBOARD RECEIVE UART	
	3800
********** (NOT USED) **********	
	13FF
RAM FOR EVEN NUMBERED COLUMNS WORK AREAS, BUFFERS, ETC.	
	1000
********** (NOT USED) **********	
	0BFF
RAM FOR ODD NUMBERED COLUMNS WORK AREAS, BUFFERS, ETC.	
	0800
********** (NOT USED) **********	
	03FF
BOTH RAM AREAS MAPPED TOGETHER	
	0000

1.0 Introduction

This monitor uses direct drive video, horizontal drive and vertical drive signals. All components except the picture tube and deflection yoke are mounted on one circuit board. All part values or part numbers are indicated on the schematic drawing.

To remove the circuit board from the terminal, first arc the high voltage lead (where it connects to the bell of the tube) to the aquadag of the tube. Do not arc to the frame of the terminal. Next disconnect the high voltage lead from the tube, disconnect the connector on the end of the neck of the tube and disconnect the horizontal and vertical yoke connectors on the circuit board. Remove the screw near the top of the board which holds the board to the power supply bracket and pull the board out of the edge connector on the display board.

2.0 Performance Specifications

2.1 Video:
- -a positive input results in a white display.
- -min. pulse width: 50 nsec.
- -rise/fall times: 20 nsec. max.
- -input impedance: 3000 ohms shunted by 50 pf.

2.2 Horizontal Drive:
- -4.0 ± 1.5 volts p.p. referred to 0 volts
- -a positive transition initiates drive
- -pulse width: 27.5 usec. nom.
- -rise/fall times: 50 nsec. max.
- -input impedance: 1000 ohms shunted by 40 pf.

2.3 Vertical Drive:
- -4.0 ± 1.5 volts p.p. referred to 0 volts.
- -a negative transition intitiates sync.
- -pulse width: 75 usec. to 1.5 msec.
- -rise/fall times: 100 nsec. max.
- -input impedance: 1000 ohms shunted by 40 pf.

2.4 Video Amplifier:
- -bandwidth: DC to 12MHz (+3db)
- -rise/fall times: 30 nsec.

2.5 Drive Frequencies:
- -horizontal: 15.75 kHz ± 500 Hz.
- -vertical: 47 to 62 Hz (automatic sync, no hold control)
- -horizontal blanking time: 10 usec. min.
- -vertical retrace time: 850 usec. min.

2.6 Display:
- -linearity: adjustable electronically in both axes.

2.7 On-board Controls:
-focus
-brightness
-horizontal linearity
-width
-vertical size
-vertical linearity
-vertical centering

2.8 Power Requirements:
- +15 volts DC
or +12 volts DC
or +12 volts DC and -5 volts DC
NOTE: The power required depends on which flyback transformer is used.

3.0 THEORY OF OPERATION

3.1 Video Amplifier:

The video input, edge connector pin 8, drives the video output stage, Q10, which drives the cathode of the tube. Zero volts on the video input turns Q10 off to give no display and a positive voltage on the video input turns Q10 on which drives the cathode of the tube to a higher voltage causing a white level on the display. Power for the collector of Q10 is generated from pin 5 of the flyback transformer, rectified into a DC voltage by D8 and then passed through R35, R36 and L1. The voltage at the collector of Q10 is approximately +80 volts DC.

The voltage from D8 also drives one end of the brightness control after it is reduced by 25 volts by zener diode D6 to approximately +55 volts. The other end of the brightness control is driven by approximately -90 volts which is generated through D5. The brightness control alters the operating point of the tube by biasing the control grid, pin 1 of the tube.

3.2 Contrast:

The contrast control is mounted on the front of the terminal as part of the power switch. The contrast control biasesthe base of Q11 between +15 volts and ground. As the contrast control is adjusted to deliber a lower voltage to Q11, Q11 turns on more and sinks more current from the video signal. This allows less current to flow through R27 causing a lower voltage at the base of Q10 and, therefore, lower video drive and less voltage to the cathode of tube.

3.3 Horizontal Deflection:

When the horizontal drive goes to logic one, Q13 saturates causing current to flow through the primary and, therefore, the secondary of driver transformer, T2. The secondary of the driver transformer drives the base of transistor, Q12, which turns the transister on, which causes current flow through the primary of the flyback transformer, T1. When the horizontal drive returns to logic zero, Q12 is cut off sharply and the flyback transformer and horizontal yoke resonate causing a large retrace pulse. Tlhe energy transfer between the flyback transformer and the horizontal yoke causes horizontal scanning of the electron beam in the tube. The width, I3, and the horizontal linearity, I2, controls, being in series with the yoke, alter the amount of current available for horizontal deflection.

The operating voltages for the tube are derived from the secondary of the flyback transformer. The signal coming from pin 7 of the flyback transformer is rectified by the EHT diode into a DC voltage of 11 to 12 KV. The other voltages are derived from the signals from pins 4 and 5 of the flyback transformer. The signal from pin 5 was covered in the video amplifier section. The signal from pin 4 is rectified into a positive voltage of approximately +750 volts DC by D7. This voltage drives one end of the focus control and the grid on pin 5 of the tube. The signal from pin 4 of the flyback transformer is also rectified into a negative voltage of approximately -90 volts DC by D5. This voltage drives one end of the focus control and of the brightness control.

3.4 Vertical Oscillator and Amplifier:

IC number U2 forms a triggered sweep oscillator. With no vertical drive signal present, it free runs at some frequency lower than the display refresh frequency. This frequency is set by R9 and C5. When the vertical drive signal is present, the falling edge of the waveform triggers the oscillator which modifies the period of its output waveform to give the display refresh frequency of either 50 or 60 Hz.

A rectangular wave is generated at pin 3 of U2 and a sawtooth wave is generated at pin 7 to provide the vertical deflection ramp. R7, Q5, D1 and D2 from a constant current source to keep the ramp linear.

The vertical deflection ramp is then buffered by IC number U1C and the vertical size control, RV2, attenuates the output from U1C.

This signal drives a power amp. consisting of U1C, Q2, Q3, Q4, Q6 and their associated resistors. This power amp. drives the top end of the vertical yoke.

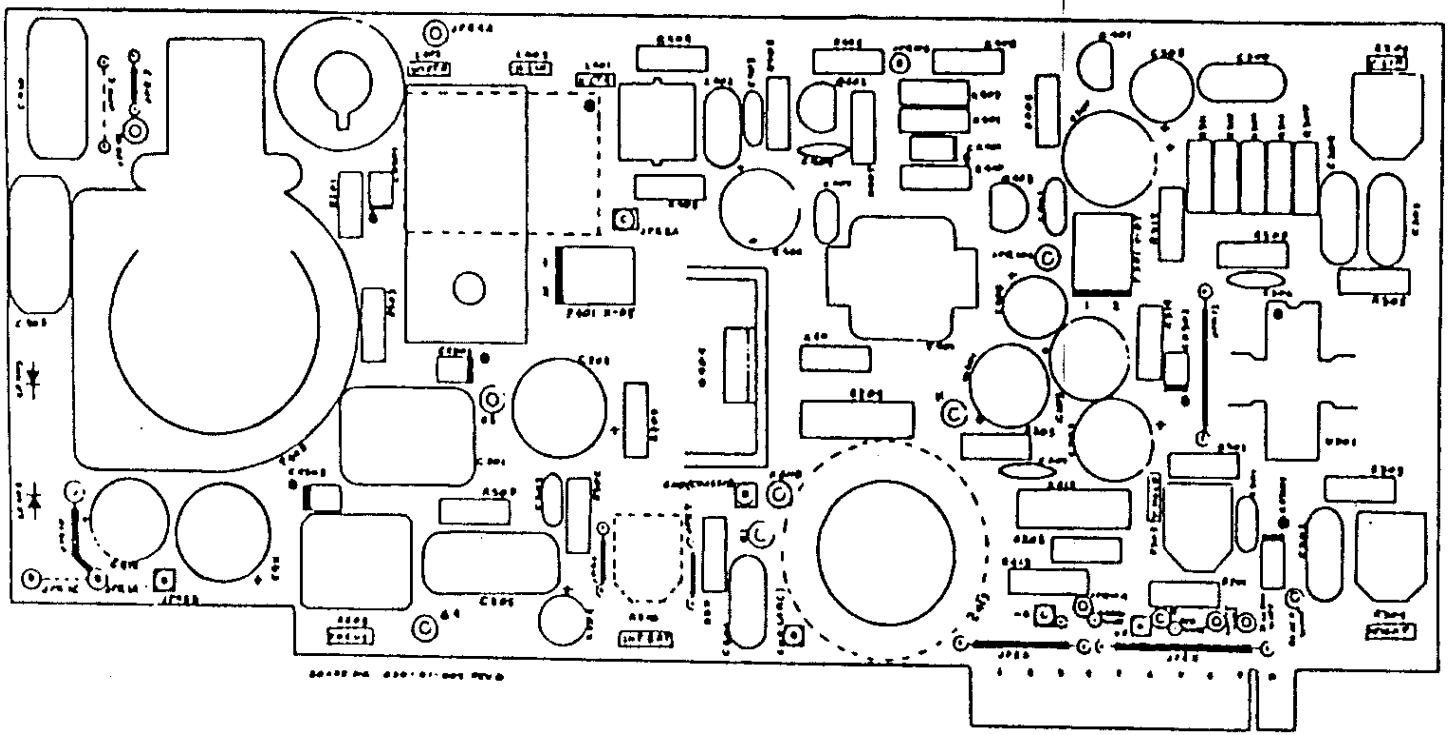
Another power amp. consisting of U1B, Q1, Q7, Q8, Q9 and their associated resistors drives the lower end of the vertical yoke.

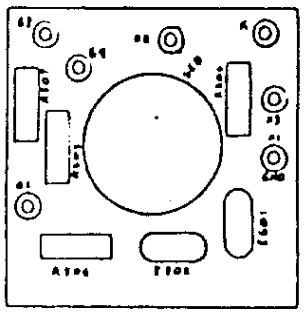
When the trace is at the top of the display, the vertical yoke is biased with approximately +7 volts on each end. The vertical deflection ramp drives the top of the yoke to +12/+15 volts causing very fast retrace to the top of the display.

The vertical center control, RV3, biases the driver for the bottom of the yoke. It changes the voltage level on the bottom of the yoke during the time that the trace is moving down the display causing the display to be moved vertically on the screen.

Because of the inductance of the yoke, the vertical deflection ramp appears at the bottom of the yoke to be slightly exponential. This wave form is fed back to the negative input of U1C and depending on the setting of the vertical linearity control, RV1, it is added or subtracted to the vertical deflection ramp to change the vertical linearity.

REVISIONS				
REV	DESCRIPTION	BY	CHKD	DATE	CHK





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ASY, MONITOR, SAM SUNG, REFERENCE

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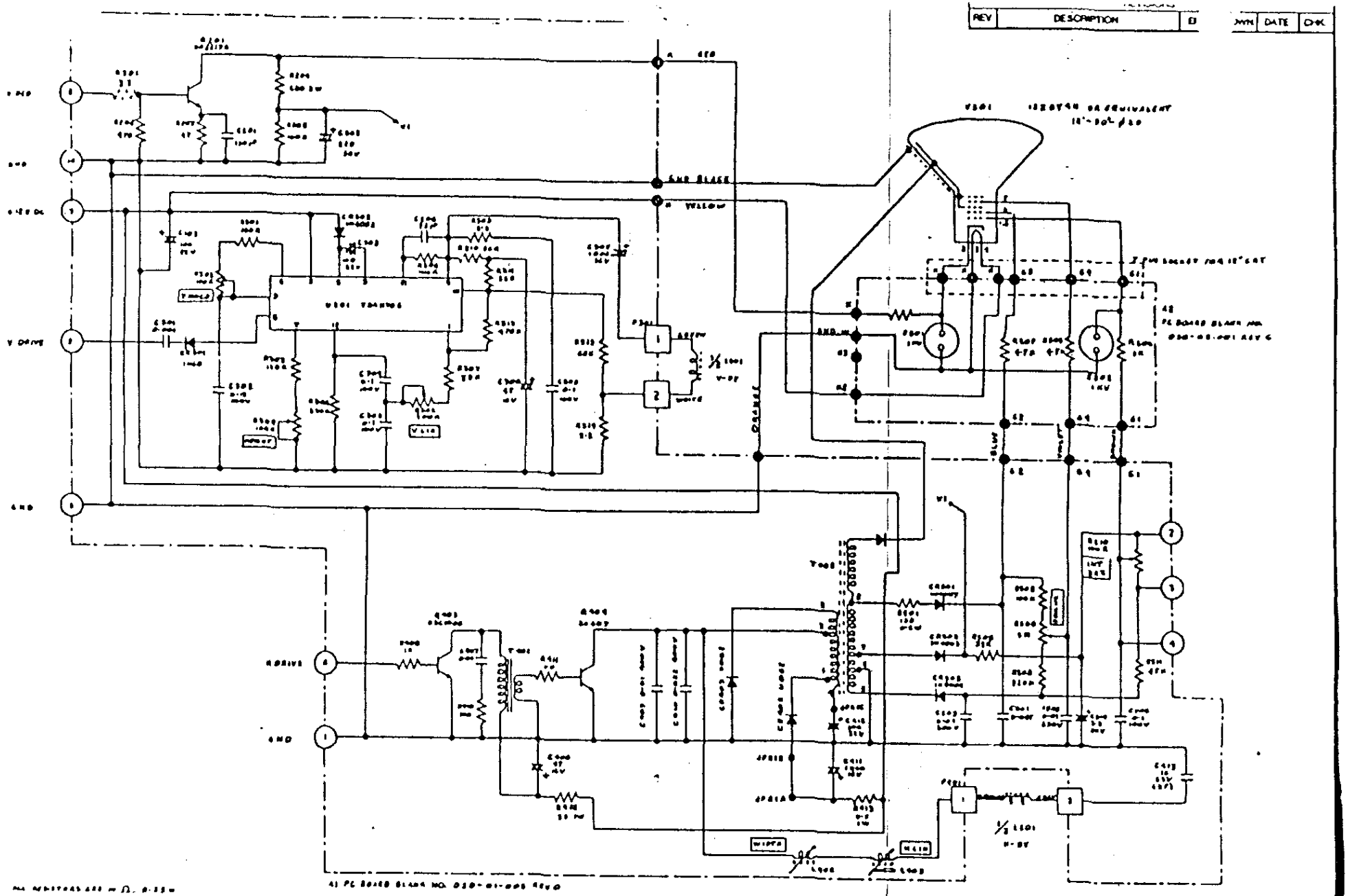
1 OF 1



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SCHEMATIC, MONITOR, 12", SAM SUNG

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